Reg. No. | | | | | | | | | |

M.E./M.TECH. DEGREE EXAMINATIONS, MAY/JUNE 2017

SECOND SEMESTER

APPLIED ELECTRONICS

AL16011 – DSP INTEGRATED CIRCUITS

(Regulation 2016)

Q. Code: 915402

Time: Three Hours **Maximum : 100 Marks**

Answer **ALL** questions

PART A - (10 X 2 = 20 Marks)

1. What are the major design steps involved in direct mapping technique in ICs?
2. Draw two input NAND gate using CMOS technology.
3. State the BIBO stable condition for LTI systems.
4. Compare 2D-DCT with FFT.
5. Show that an FIR interpolator can be decomposed into L parallel FIR filters that operate at the input sampling rate and produce a combined output signal with L times higher sampling rate.
6. List the finite word length effects in Digital filters.
7. Why complex PEs are preferred in DSP processors?
8. Draw the ideal DSP architecture.
9. List out the benefits of redundant number system.
10. What is Cordic algorithm and where it is used?

PART B - (5 X16 = 80 Marks)

11. (a) Write short note on the following

    (i) Recent trends in CMOS technology (8)

    (ii) ASIC for DSP system (8)

(OR)

(b) (i) Explain VLSI process technologies in detail. (10)

(ii) Compare CMOS and Bipolar Technology. (6)

12. (a) Find DFT for the following sequences and hence find X(8)

(i) $x(n) = \{ (0.5)^n \quad n=0,1,2,3,4$ (8)
$= 0 \quad n=5,6,7,\ldots\ldots\ldots..15\}$

(ii) $x(n) = \{1 \quad n=0,1,2,3$ (8)
$0 \quad n=4,5,6,7$
$0.5 \quad n=8,\ldots\ldots..15\}$

(OR)

(b) (i) Define sampling of analog signals and explain the procedure to select sampling frequency with suitable example. (10)

(ii) Draw signal flow graph of $y(n)=ay(n-1)+x(n)+bx(n-1)-cx(n-2)+dy(n-2)$. (6)

13. (a) For an Analog system transfer function $H_a(s)=(s+2) / (s^2+2s+10)$, determine H(z) by

(i) Impulse Invariant Transformation (8)

(ii) Bilinear Transformation (8)

(OR)

(b) The transfer function of a system is provided by (16)
$H(z)=(1+z^{-1}) / (1-0.5z^{-1})(1-z^{-1}+z^{-2})$. Realize the system in Direct, Cascade and Parallel Structure.

14. (a) Explain in detail the various steps involved in mapping DSP Algorithm to Hardware. (16)

(OR)

(b) (i) Discuss the Implementation of Complex PE into Hardware (10)

(ii) What are the Benefits of Serial Adder Compound to Parallel Adder system (6)

15. (a) Draw Layout of FFT Processor and discuss its operation in detail. (16)

(OR)

(b) What is DCT Processor? Explain its Algorithm which is followed in the Processor. (16)