Q. Code: 908929

Reg. No. | | | | | | | | | |

M.E. / M.TECH. DEGREE EXAMINATIONS, DEC 2019

First Semester

CP18102 – ADVANCED COMPUTER ARCHITECTURE

(Common CP & NW)

(Regulation 2018)

Time: Three Hours **Maximum : 100 Marks**

Answer **ALL** questions

PART A - (10 X 2 = 20 Marks)

		CO	RBT
1.	Define MIPS and MIPS Rate.	**1**	**R**
2.	Write the CPU performance equation and define CPI.	**1**	**U**
3.	Which memory is called asynchronous DRAM?	**2**	**U**
4.	How will you calculate Average memory access time?	**2**	**U**
5.	List the demerits of symmetric shared memory.	**3**	**U**
6.	Why do we need synchronization in a multiprocessor?	**3**	**U**
7.	Define CMT.	**4**	**R**
8.	List the Intel Multicore technologies.	**4**	**U**
9.	Write the difference between CPU and GPU.	**5**	**U**
10.	What is meant by Loop level parallelism?	**5**	**R**

PART B - (5 X16 = 80 Marks)

11.	(a)	Illustrate with a neat sketch about the functional components of a digital computer system.	**(16)**	**1**	**AP**
		(OR)			
	(b)	(i) Illustrate the concept of ILP with different types of dependencies in ILP with examples.	**(10)**	**1**	**AP**
		(ii) Some microprocessors that are designed to have adjustable voltage, so a 17% reduction in voltage may result in a 17% reduction in frequency. What would be the impact on dynamic energy and on dynamic power?	**(6)**	**1**	**AP**

12.	(a)	Discuss in detail about various hit time reduction and miss penalty techniques to improve cache performance.	**(16)**	**2**	**U**
		(OR)			
	(b)	Discuss in detail about the various memory technologies.	**(16)**	**2**	**U**
13.	(a)	Explain the concept of distributed shared memory along with directory based cache coherence protocols with an example.	**(16)**	**3**	**U**
		(OR)			
	(b)	(i) Write the importance of memory consistency model and illustrate the types in detail with examples.	**(10)**	**3**	**U**
		(ii) Write short notes on Crossbar Network.	**(6)**	**3**	**U**
14.	(a)	(i) Explain in detail about the architectural features of IBM Cell processor with a neat diagram.	**(10)**	**4**	**U**
		(ii) Compare Homogeneous and Heterogeneous multi-core architectures.	**(6)**	**4**	**AN**
		(OR)			
	(b)	(i) State and explain the necessary design factors for warehouse scale computers.	**(8)**	**4**	**U**
		(ii) How will you measure the cost and efficiency of a warehouse scale computers? Explain in detail.	**(8)**	**4**	**AN**
15.	(a)	Discuss in detail about Vector Architectures of Data – level parallelism with a neat block diagram.	**(16)**	**5**	**U**
		(OR)			
	(b)	Discuss in detail about Graphics Processing Units and its programming with a neat example.	**(16)**	**5**	**U**