Q. Code: 899687

M.E. / M.TECH. DEGREE EXAMINATIONS, DEC 2020 (Held during April, 2021)

First Semester

CP18102 – Advanced Computer Architecture

(Common to CS & NW)

(Regulation 2018)

Time: Three hours Maximum : 80 Marks

Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. Given Fraction $_{enhanced}$ = 0.4, Speedup $_{enhanced}$ =10, Waiting time for IO=60% of the time. Overall speedup = ?
   a. 1.48 b. 1.56 c. 10.4 d.6.4

2. In way prediction, extra bits are kept in the _____ to predict the way or block within the set of next _____ access.
   a. Register, cache
   b. Cache, cache
   c. Cache, register
   d. Memory, cache

3. Given cache size= 32 KB, block size=64, set associativity = 4. How many number of bits does the instruction cache index has?
   a. 10 bits
   b. 128 bits
   c. 7 bits
   d. 32 bits

4. Tomasulo's scheme resolves WAR hazards using _____
   a. Source operand buffering
   b. Destination operand buffering
   c. Both source and destination operand buffering
   d. None of the above

5. Number of convoy=m; Number of Chimes=m
   For a length of vector:n , number of clock cycles required is _____
   a. m^2 b. m x n c. n^2 d. m+n

6. When a code is said to be vectorized or vectorizable?
7. Use the GCD test to determine whether dependencies exist in the following loop

```
(for (i=0; i<100; i=i+1)
 {
X[2*i+3] = X[2*i] * 5.0;
}
```

8. When can we have a paired single operation?

PART B - (4 X16 = 64 marks)

09. (a) (i) The following table illustrate the different classes of Instructions. **(8)**

Class	**A**	**B**	**C**
CPI for class	2	3	3
IC in sequence 1	2	1	2
IC in sequence 2	4	1	2

- Which code sequence executes the most instructions?
- Which will be faster?
- What is the CPI for each sequence?

(ii) How can we extend Tomasulo's algorithm to handle speculation? Compare about the additional units required along with the purpose in detail. **(8)**

(OR)

(b) Suppose we have a VLIW that could issue two memory references, two FP operations, and one integer operation or branch in every clock cycle. Show an unrolled version of the loop element[i] = element[i] + z for such a processor. Unroll as many times as necessary to eliminate any stalls. Ignore delayed branches. **(16)**

10. (a) Can we provide Protection via Virtual Memory? Justify your points with suitable architecture. **(16)**

(OR)

(b) As multiple processors operate in parallel, and independently multiple caches may possess different copies of the same memory block. How can you handle them? **(16)**

11. (a) Analyze the different types of interconnection networks. Bring out the suitability of each in real time applications with examples. **(16)**

(OR)

(b) Discuss about the Similarities and Differences between Vector Architectures and GPUs. **(16)**

12. (a) Do WSC supports all the goals and requirements of server architects? Justify your answer with suitable examples. **(16)**

(OR)

(b) How the vector processor works for the following double-precision instruction? **(16)**

$Y = a \times B + Y$