Reg. No. | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATIONS, MAY 2017

SECOND SEMESTER

CS16201 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to CS and IT)

(Regulation 2016)

Q. Code: 960189

Time: Three hours **Maximum : 100 marks**

Answer **ALL** questions

PART A - (10 X 2 = 20 Marks)

1. Convert the decimal number 9 to Excess-3 and Gray code.
2. State DeMorgan's laws.
3. Implement 8:1 MUX using 4:1 MUX.
4. Realize the function Y=∑m(1,4,6) using suitable decoder.
5. Draw the logic diagram for T flipflop.
6. Convert SR to T flip flop.
7. What is meant by race in asynchronous sequential circuit?
8. Enumerate the fundamental mode of operation in asynchronous sequential circuit.
9. Compare SRAM and DRAM.
10. What is ASIC?

PART B - (5 X16 = 80 Marks)

11. (a) (i) Simplify the expression Z=AB+AB'.(A'C')' **(4)**

(ii) Express function F(A, B, C, D)=D(A'+B)+B'D in product of maxterms. **(4)**

(iii) Reduce the function using K-map technique **(8)**
f(A,B,C,D)=∑m(1,3,5,8,9,11,15)+d(2,13)

(OR)

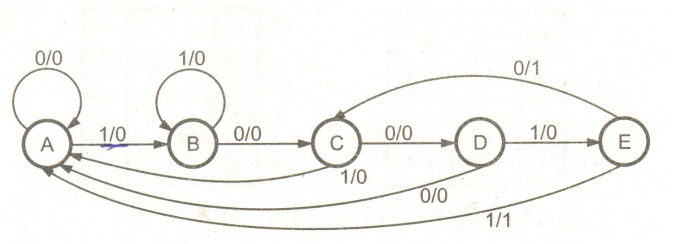
(b) Using tabulation method and 'K'map simplify the function **(16)**
f(W,X,Y,Z)= πM (0,4,5,9) . d(1,7,13)

12. (a) Implement the function using 8:1 multiplexer **(16)**
f(a,b,c,d)= ∑m(0,2,6,10,11,12,13)+d(3,8,14). Write HDL simulation code for the same.

(OR)

(b) Design a 4-bit ripple carry adder/subtractor. Discuss in detail about carry lookahead adder. **(16)**

13. (a) For the state diagram given below design a sequential circuit using D flip-flops. **(16)**



(OR)

(b) (i) With a neat diagram explain about master slave JK flip flop. **(8)**

(ii) Design a divide by 6 counter using T-flip flop. **(8)**

14. (a) (i) An asynchronous sequential circuit has two internal states and one output. The excitation and output function describing the circuit are as follows **(8)**

$Y_1=x_1x_2+x_1y_2+x_2y_1$

$Y_2=x_2+x_1y_1y_2+x_1y_1$

$Z=x_2+y_1$

Draw the logic diagram of the circuit.

(ii) Derive the transition table and output map. **(8)**

(OR)

(b) Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. When $X_1=0$, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0. **(16)**

15. (a) (i) Write short notes on memory decoding. **(8)**

(ii) Design a combinational circuit using ROM. The circuit accepts 3 bit number and generates an output binary number equal to square of the input number. **(8)**

(OR)

(b) Design BCD to gray code converter and implement using PLA. **(16)**