Q. Code: 359375

Reg. No. | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATIONS, DEC 2019

Third Semester

EC16301 – DIGITAL ELECTRONICS

(Electronics and Communication Engineering)

(Regulation 2016)

Time: Three Hours **Maximum : 100 Marks**

Answer **ALL** questions

PART A - (10 X 2 = 20 Marks)

		CO	RBT
1.	State De-Morgan's theorem.	1	R
2.	Express the function $Y = A + B^1C$ in canonical POS.	1	AP
3.	What is encoder?	2	R
4.	List few applications of Multiplexer.	2	R
5.	What are the classifications of sequential circuits?	3	R
6.	How many flip-flops are required to build a binary counter that counts from 0 to 2047?	3	AP
7.	What is memory decoding?	4	R
8.	What are the different types of programmable logic devices?	4	R
9.	What are hazards?	3	R
10.	Define non critical race.	3	R

PART B - (5 X16 = 80 Marks)

11.	(a)	(i)	Minimize the following logic function using K- map and realize using NAND and NOR gates. $F(A,B,C,D) = \sum m(1,3,5,8,9,11,15) + d(2,13)$	**(10)**	**1**	**AP**
		(ii)	Realize NOT, OR, AND gates using Universal gates.	**(6)**	**1**	**AP**
			(OR)			
	(b)		Simplify the given switching function using Quine - McCluskey method $F(W, X, Y, Z) = \sum m(0,5,7,8,9,10,11,14,15)$ and implement using only NOR gates.	**(16)**	**1**	**AP**

12.	(a)	Design a BCD adder and explain its working with necessary circuit diagrams.	**(16)**	**2**	**AP**
		(OR)			
	(b)	(i) Design a 4-bit binary parallel adder and explain the same.	**(8)**	**2**	**AP**
		(ii) Design a 3 : 8 decoder using basic gates.	**(8)**	**2**	**AP**
13.	(a)	(i) Design a 3-bit universal shift register and explain its operation.	**(8)**	**3**	**AP**
		(ii) Design a 3-bit Parallel in Serial Out (PISO) shift register and explain its operation.	**(8)**	**3**	**AP**
		(OR)			
	(b)	Design a 4-bit Asynchronous Ripple counter and explain its operation with timing diagrams.	**(16)**	**3**	**AP**
14.	(a)	(i) Compare and contrast the features of TTL and CMOS logic families.	**(8)**	**4**	**U**
		(ii) Draw the circuit diagram and explain the operation of 2 input TTL NAND gate with Totem-pole output.	**(8)**	**4**	**U**
		(OR)			
	(b)	Write notes on			
		1. PAL	**(8)**	**4**	**U**
		2. PLA	**(8)**	**4**	**U**
15.	(a)	Design a asynchronous sequential circuit that has 2 inputs x_1 and x_2 and one output z. When $x_1 = 0$, output is 0. The change in x_2 that occurs while x_1 is 1 will cause output z =1. The output z will remain 1 until x_1 returns to 0.	**(16)**	**3**	**AP**
		(OR)			
	(b)	Explain the different methods of Race free state assignment.	**(16)**	**3**	**AP**