Q. Code: 243180

Reg. No. | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATIONS, DEC 2019

Fourth Semester

EE16403 – Digital Logic Circuits

(Electrical and Electronics Engineering)

(Regulation 2016)

Time: Three Hours **Maximum : 100 Marks**

Answer **ALL** questions

PART A - (10 X 2 = 20 Marks)

		CO	RBT
1.	Simplify f = (b + bc) (b + b'c) (b+d).	1	AP
2.	Construct an OR gate using universal NAND gates.	1	AP
3.	Sketch the logic diagram of 8 : 3 encoder circuit.	2	AP
4.	Realize a half adder using VHDL coding.	2	AP
5.	State the truth table of JK flip flop and T flip flop.	3	R
6.	Estimate the type of Mod counters used to display minutes in digital clock.	3	AN
7.	What is flow table and primitive flow table?	3	R
8.	Compare sequential and combinational circuits.	3	U
9.	Develop a simple Inverter logic using NPN Transistor.	5	AP
10.	Define Fan-out and Fan-in.	5	R

PART B - (5 X16 = 80 Marks)

11.	(a)	(i)	Simplify the Boolean function using map method and implement using universal gates $F(w,x,y,z) = \sum m(1,3,5,6,7,8,12,14) + d(9,15)$	**(8)**	**1**	**AP**
		(ii)	Reduce the following expression using K-map and implement using logic gates. $f = x'y'z+w'xz+wxy'+wxz+ w'xyz$	**(8)**	**1**	**AP**
			(OR)			
	(b)	(i)	State and prove Demorgan's theorem.	**(6)**	**1**	**U**
		(ii)	List various binary codes used in digital systems and explain any two binary codes with suitable illustrations.	**(10)**	**1**	**U**
12.	(a)	(i)	Design and implement using logic gates 4-bit Gray to Binary code converter.	**(8)**	**2**	**AN**
		(ii)	Design a full subtractor circuit with three inputs A, B, C and two outputs D and B. Implement the circuit using universal gates.	**(8)**	**2**	**AN**
			(OR)			
	(b)	(i)	Design a 4 bit even parity generator.	**(8)**	**2**	**AN**

	(ii)	Implement the following Boolean function using 8:1 Multiplexer F(A,B,C,D) = Σm(0,1,3,4,8,9,15)	**(8)**	**2**	**AP**
13.	(a)	Draw the state diagram from the present state – Next state table given. Also, apply state minimization technique to reduce the number of states in the following:	**(16)**	**3**	**AP**

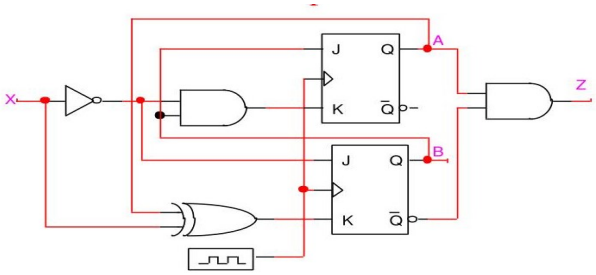
Present state	Next state		Output	
	$x=0$	$x=1$	$x=0$	$x=1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

(OR)

	(b)	Design MOD 10 synchronous counter using JK flip flop.	**(16)**	**3**	**AN**
14.	(a)	(i) Explain in detail the cycles and races in asynchronous sequential design circuit.	**(10)**	**3**	**U**
		(ii) Design a hazard free circuit for the given Boolean function F = ∑m(1,3,6,7,13,15)	**(6)**	**3**	**AN**

(OR)

	(b)	Analyse the given synchronous sequential circuit and obtain its state diagram	**(16)**	**3**	**AN**



15.	(a)	Derive the PLA programming table for the boolean function combinational circuit. Minimize the number of product terms and implement using PLA programming device. F1 = ∑m(0,1,2,3,4,7,8,11,12,15) F2 = ∑m(2,3,6,7,8,9,12,13) F3 = ∑m(1,3,7,8,11,12,15) F4 = ∑m(0,1,4,8,11,12,15)	**(16)**	**4**	**AP**

(OR)

	(b)	Enumerate the different logic families used to fabricate digital gate ICs. Draw and Explain the NOR / OR Logic using Emitter Coupled Logic.	**(16)**	**5**	**U**