Q. Code: 170509

Reg. No. | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATIONS, DEC 2019

Third Semester

IT16301 – COMPUTER ORGANIZATION AND ARCHITECTURE

(Information Technology)

(Regulation 2016)

Time: Three Hours **Maximum : 100 Marks**

Answer **ALL** questions

PART A - (10 X 2 = 20 Marks)

		CO	RBT
1.	What is the use of Accumulator register?	**1**	**R**
2.	What is an effective address?	**1**	**R**
3.	Draw the format for single precision for IEEE 754 standard?	**2**	**U**
4.	What is the difference between polish and reverse polish notation?	**2**	**U**
5.	Explain briefly how to overcome data hazard in pipeline architecture.	**3**	**AP**
6.	Differentiate interrupt and exception.	**3**	**U**
7.	What is a programmed i/o?	**4**	**R**
8.	Write the formula to measure cache performance.	**4**	**R**
9.	What is the function of GPU.	**5**	**U**
10.	What is Uniform memory access and Non uniform memory access?	**5**	**U**

PART B - (5 X16 = 80 Marks)

11.	(a)	Design a basic computer with a neat diagram.	**(16)**	**1**	**AP**
		(OR)			
	(b)	Explain in detail arithmetic and shift operation with a neat diagram.	**(16)**	**1**	**AP**
12.	(a)	Draw the flowchart for Booth multiplication and solve -4*2 using Booth multiplication algorithm.	**(16)**	**2**	**AP**
		(OR)			
	(b)	Draw the flowchart for floating point multiplication and solve 0.5 * 0.4375 using floating point multiplication algorithm.	**(16)**	**2**	**AP**

13.	(a)	Explain and draw the complete datapath with control signals for R type I type and J type instruction.	**(16)**	**3**	**AP**
		(OR)			
	(b)	Explain the concept of Pipelining and explain various hazards in pipeline.	**(16)**	**3**	**AP**
14.	(a)	Explain how DMA is used for direct transfer of data between memory and peripherals.	**(16)**	**4**	**U**
		(OR)			
	(b)	Explain in detail the working of virtual memory, various types of virtual memory available and how to implement TLB in virtual memory with necessary block diagram.	**(16)**	**4**	**U**
15.	(a)	Explain in detail Flynn classification of parallel hardware.	**(16)**	**5**	**AP**
		(OR)			
	(b)	Explain in detail various hardware multithreading models with a neat diagram.	**(16)**	**5**	**AP**