B.E./B.TECH. Degree Examination, December 2020

Second Semester

CS16201 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Regulation 2016)

Time: Three hours Maximum : 80 Marks

Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. The NAND gate output will be zero if the two inputs are

   (A) 00 (B) 01 (C) 10 (D) 11

2. A full adder logic circuit will have

   (A) Two inputs and one output. (B) Three inputs and three outputs.

   (C) Two inputs and two outputs. (D) Three inputs and two outputs.

3. SR Flip flop can be converted to T-type flip-flop if ?

   (A) S is connected to Q (B) R is connected to Q

   (C) Both S and R are shortend (D) S and R are connected to Q and Q' respectively

4. The type of register in which data is entered into it only one bit at a time, but has all data bits

   (A) Serial in serial out register (B) Parallel in serial out register

   (C) Serial in parallel out register (D) Parallel in parallel out register

5. Convert $(56.333)_7 = (\quad)_8$

6. In what way an encoder differs from a decoder?

7. For a 8K X 16 memory unit, state the number of address lines, input lines and output lines are needed.

8. Where a volatile memory cannot be deployed?

PART B - (4 X16 = 64 marks)

9. (a) Simplify the Boolean function using K-map and implement using gates. **(16)**

   $F(w,x,y,z)=\sum m(0,2,4,6,8) + \sum d(10,11,12,13,14,15)$

   (OR)

   (b) Using Tabulation method simplify the Boolean function $F(w,x,y,z) = m(0,2,3,5,7,9,11,13,14,16,18,24,26,28,30)$. **(16)**

10. (a) Implement a combinational circuit such that given a binary number it has to produce its equivalent gray code. **(16)**

    (OR)

    (b) Design a 8 X 1 MUX for the following function: **(16)**

    $F(A,B,C,D) = \sum (1,2,4,5)$

    $F(A,B,C,D) = \sum(0,1,3,4,8,9,15)$

11. (a) An asynchronous sequential circuit has two internal states and one output. The two excitation and output function are as follows: **(16)**

$Y_1 = x_1x_2 + x_1y'_2 + x'_2y_1$

$Y_2 = x_2 + x_1y'_1y_2 + x'_1y_1$

$z = x_2 + y_1$

Draw the logic diagram of the circuit.

Derive the transition table and the output map.

Describe the behavior of the circuit.

(OR)

(b) Design a binary counter using T-flip-flops to count in the following sequences: **(16)**

000,001,010,011,100,101,110,111,000

12. (a) A sequential circuit with two D flip-flops A and B, two inputs x and y and one output is specified by the following next-state and output equations **(16)**

A(t+1)=x'y+xB

B(t+1)=x'A+xB

z=A

Draw the logic diagram of the circuit.

List the state table for the sequential circuit.

Draw the corresponding state diagram.

(OR)

(b) Implement the following function using PLA **(16)**

$A(x,y,z)=\sum m(1,2,4,6)$

$B(x,y,z)=\sum m(0,1,6,7)$

$C(x,y,z)=\sum m(2,6)$