B.E./B.TECH. Degree Examination, December 2020

Third Semester

EC16301 – Digital Electronics

(Regulation 2016)

Time: Three hours Maximum : 80 Marks

Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. For an n-variable Boolean funciton, K-map contains ____ .
   a)n cells b)2n cells c)2^n cells d)4n cells
2. Which of the following is correct for full adders?
   a) Full adders have the capability of directly adding decimal numbers
   b) Full adders are used to make half adders
   c) Full adders are limited to inputs since there are only two binary digits
   d) In a parallel full adder, the first stage may be a half adder
3. How many address lines are required to design 32 x 8 bit RAM?
   (a) 8 (b) 32 (c) 5 (d) 10
4. In Verilog HDL, bit-wise operator used to perform AND operation is
   (a) & (b) ^ (c) ~ (d) |
5. Suggest a flip flop which overcomes the problem of race around condition. Justify your answer.
6. Give the significance of priority encoder.
7. Compare SRAM with DRAM.
8. Realize an 8x1 multiplexer using 2x1 multiplexer.

PART B - (4 X16 = 64 marks)

09. (a) (i) Simplify the given Boolean function using K-Map. **(10)**
    Y (A, B, C, D) = ∑m (**0,1,2,5,6,7,8,9,10,14**).
    (ii) Obtain the canonical product of sums for the Boolean expression **(6)**
    F = **A + B'C**

    (b) Determine the minimal sum of products for the Boolean function using tabulation method. F(A,B,C,D) = ∑m (**1,3,4,5,9,10,11**) +∑d (**6,8**) **(16)**

10. (a) Construct a 4-bit carry look ahead adder circuit and discuss its advantages over parallel binary adder. **(16)**

    (b) (i) Design a digital circuit that decodes a 3-bit input into 8-bits. **(8)**
    (ii) Design a 4-bit even parity checker. **(8)**

11. (a) (i) Discuss the working of T flip flop with a neat diagram. Also draw its characteristic table and excitation table. **(8)**

(ii) Suggest suitable 4-bit shift registers which shift the input from left to right (a) serially bit by bit (b) parallel **(8)**

(b) Design a 4-bit asynchronous down counter using JK flip flop and draw its timing diagram. **(16)**

12. (a) Design a PLA structure for the following functions. **(16)**

F1 = Σm(**5,7,10,14,15)**

F2 = Σm **(6,7,9,13,15)**

(b) (i) Write a Verilog HDL code to implement 1 x 8 demultiplexer. **(8)**

(ii) Obtain a static hazard free circuit for the following switching function F = Σm (**1,3,5,7**) **(8)**