B.E./B.TECH. Degree Examination, December 2020

Seventh Semester

EC16703 Embedded and Real Time Systems

(Regulation 2016)

Time: Three Hours Maximum:80 Marks

Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. The Logical Instructions are: ORR, EOR, TEQ, AND, TST, BIC, MOV, MVN. Why is the V flag unaffected by the logical data processing instructions?

   a) Since V flag and C flag are always the same after any logical operations

   b) Because it will delay the execution of logical operations

   c) V flag is relevant only when an Arithmetic operation is performed

   d) None of the above

2. Suppose three periodic tasks with execution times of 20 millisecond,30 millisecond, and 40 millisecond, and periods of 150 millisecond, 250 millisecond, and 350 millisecond are to be run using a basic table-driven scheduler. What is the minimum time period for which the task schedule should be stored in a schedule table?

   (a) 750 milliseconds

   (b) 120 milliseconds

   (c) 80 milliseconds

   (d) 5250 milliseconds

3.

1. IoT smart appliance	(i) sensors + network + database + dashboard
2. IoT monitoring system	(ii) connected appliance + network + UI
3. IoT control system	(iii) sensors + network + database + controller + actuator

   a 1-iii, 2-ii, 3-i

   b 1-ii, 2-iii, 3-i

   c 1-ii, 2-i, 3-iii

   d 1-iii, 2-ii, 3-iii

4. Which model is based on successive refinement approach?

   (a) Waterfall model

   (b) Elliptical model

   (c) Spiral Model

   (d) None

5. Differentiate top-down and bottom-up embedded system design.

6. Compare GPOS versus RTOS.

7. Analyze the advantages of CRC card in the design of system architecture.
8. Justify the need for software modem.

PART B - (4 X16 = 64 marks)

09. (a) Analyze the requirements for designing a GPS moving map in embedded system design process. **(16)**

(OR)

(b) How fast can the CPU execute instructions? Illustrate how pipe lining and caching can substantially influence CPU performance? **(16)**

10. (a) (i) Illustrate circular queues and buffers in embedded systems for signal processing. **(10)**

(ii) Interpret the Windows CE RTOS Interrupts with a sequence diagram. **(6)**

(OR)

(b) (i) Compare the principle, merits and limitations of inter-process communication mechanisms. **(10)**

(ii) Illustrate rate monotonic scheduling. **(6)**

11. (a) Interpret the rationale behind the design methodologies and design flows involved in the design of complex real time embedded systems. **(16)**

(OR)

(b) (i) Illustrate why MPSoCs are preferred over general purpose microprocessors. **(8)**

(ii) Differentiate between accelerator and co-processor. Analyze the performance of accelerators in terms of the speed up factor. **(8)**

12. (a) Demonstrate data compressor and software modem. **(16)**

(OR)

(b) Design a telephone answering machine that includes requirements, software, system architectures, component design, testing and system integration. **(16)**