B.E./B.TECH Degree Examination, December 2020

Fourth Semester

EE16403-DIGITAL LOGIC CIRCUITS

(Regulation 2016)

Time: Three hours Maximum : 80 Marks

Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. The Octal equivalent of the HEX number AB.CD is
   a. 253.314_8
   b. 253.632_8
   c. 526.314_8
   d. 526.632_8
2. A Combinational circuit
   a. Always contains memory elements
   b. Never contains memory elements
   c. May sometimes contain memory elements
   d. Contain only memory elements
3. Which of the following is correct for a gated D-type flip-flop?
   a. The Q output is either SET or RESET as soon as the D input goes HIGH or LOW
   b. The output complement follows the input when enabled
   c. Only one of the inputs can be HIGH at a time
   d. The output toggles if one of the inputs is held HIGH
4. A condition occur when an Asynchronous sequential circuit changes two or more binary state variables
   a. Deadlock condition
   b. Running condition
   c. Race condition
   d. No change condition
5. Construct the given expression in canonical SOP form Y = AC + AB + BC using only NOR gate.
6. Draw the logic diagram of adder circuit for 3 bit inputs.
7. Draw a 4 bit shift register used in a serial output port.
8. Write VHDL coding for 4 X 1 Multiplexer.

PART B - (4 X16 = 64 marks)

9. (a) (i) State and prove DeMorgan's theorems. **(4)**
   (ii) Simplify the Boolean Expression F = πM(0,3,4,7,8,10,12,14) + d(2,6). Also realize the expression with logic gates. **(12)**

(OR)

(b) (i) Write short notes on Alphanumeric codes. **(4)**

(ii) Simplify the given function and implement in NAND-NAND logic. **(12)**

$F= \sum m(1,3,5,6,7,8,12,14) + \sum d(9,15)$

10. (a) Design a Gray to Binary code converter with neat sketch. Examine any one 4-bit gray code to binary code conversion. **(16)**

(OR)

(b) (i) Implement the following Boolean function using 8X1 multiplexer. **(8)**

$F(A,B,C,D)=\sum m(0,2,3,5,9,10,12,14,15)$

(ii) Explain with neat sketch 3:8 Decoder logic circuit. **(8)**

11. (a) Design a synchronous Mod-12 up counter using JK flip-flops. **(16)**

(OR)

(b) A sequential circuit has 2D ff's A and B an input x and output y is specified by the following next state and output equations. **(16)**

A (t+1)= Ax + Bx

B (t+1)= A'x

Y= (A+B) x'

(i) Draw the logic diagram of the circuit.

(ii) Derive the state table.

(iii) Derive the state diagram

12. (a) Design an Asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. When X_1=0, the output Z is 0. The first change in X_2 that occurs while X_1 is '1' will cause output Z to be '1'. The output Z will remain '1' until X_1 returns to zero is '0'. **(16)**

(OR)

(b) Draw the Logic diagram, transition table and primitive flow table for the expression given below **(16)**

$$X_1^+ = X_0 I_1 + I_0 X_1$$
$$X_0^+ = X_0 I_1 + \overline{X_1}\,\overline{I_1} I_0 + \overline{X_1} X_0 I_1$$
$$Z = X_0 I_1$$