Q.CODE:494029

Reg. No. | | | | | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATIONS, MAY 2023

Third Semester

AD18201 – DIGITAL LOGIC DESIGN

(Regulation 2018/2018A)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Perform arithmetic operations in any number system & to simplify the Boolean expression using K –Map and Tabulation techniques	**2**
CO 2	Use Boolean Simplification techniques to design a combinational hardware circuit & Design and analysis of a given digital	**3**
CO 3	Design and analysis of a given digital Sequential hardware circuit	**4**
CO 4	Design and analysis of a given digital asynchronous sequential circuits	**4**
CO 5	Design using PLD	**4**

PART- A (10 x 2 = 20 Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Convert (0.6875) to binary	**1**	**2**
2.	Draw the truth table of Ex-OR gate	**1**	**2**
3.	Draw the circuit of full adder	**2**	**2**
4.	What is multiplexing	**2**	**2**
5.	Compare latches and flip flops	**3**	**3**
6.	Compare Sequential and combinational circuit	**3**	**3**
7.	What is flow table	**4**	**2**
8.	Define critical races	**4**	**2**
9.	List the different types of ROM	**5**	**2**
10.	Draw the structure of a memory cell	**5**	**2**

PART- B (5 x 14 = 70 Marks)

		Marks	CO	RBT LEVEL
11. (a)	Implement the following using only NAND gates F(a,b,c,d,) = Pi (0,2.5.8.9.13)	**(14)**	**1**	**4**
	(OR)			
(b)	Simplify using Quine Mc clusky Method F(A,B,C,D) = (0,2,3,5,7,9,11,12) + d(1,4,10)	**(14)**	**1**	**4**

12. (a)	Design a decimal adder circuit.	**(14)**	**2**	**3**
	(OR)			
(b)	Design a multiplexer circuit for the boolean function F(A,B,C,D) = (1,3,4,11,12,13,14,15)	**(14)**	**2**	**3**
13. (a)	Explain in detail about universal shift register	**(14)**	**3**	**4**
	(OR)			
(b)	With a neat diagram explain the working of johnson counter	**(14)**	**3**	**4**
14. (a)	Discuss in detail about the various types of hazards	**(14)**	**4**	**3**
	(OR)			
(b)	Design a gated latch circuit with two inputs *G* (gate) and *D* (data), and one output *Q*. Binary information present at the D input is transferred to the Q output when G=1.The Q output will follow the D input as long as G=1. When G goes to 0,the information that was present at the D input at the time the transition occurred is retained at the Q output.	**(14)**	**4**	**3**
15. (a)	Using ROM, implement a combinational circuit which accepts a 3 bit number and generates an output binary number equal to the square of the input number.	**(14)**	**5**	**3**
	(OR)			
(b)	Discuss in detail about the various error detection and correcting codes.	**(14)**	**5**	**3**

PART- C (1 x 10 = 10 Marks)

(Q.No.16 is compulsory)

		Marks	CO	RBT LEVEL
16.	Design and implement a BCD to Excess3 code convertor circuit	**(10)**	**2**	**5**