Q. Code:478450

Reg. No.

B.E. / B.TECH. DEGREE EXAMINATIONS, MAY 2023
Third Semester
CS18201 – DIGITAL PRINCIPLES AND SYSTEM DESIGN
(Computer Science and Engineering)
(Regulation 2018/2018A)

TIME: 3 HOURS   MAX. MARKS: 100

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Students will be able to learn the different types of number systems and simplification of Boolean functions.	2
CO 2	Students will be able to understand various logic gates and their usage.	3
CO 3	Students will be able to study, analyse and design various combinational circuits and its implementation using VHDL.	4
CO 4	Students will be able to study, analyse and design various synchronous and asynchronous sequential circuits and its implementation using VHDL.	4
CO 5	Students will be able to understand the different type of memory and their structures.	4

PART- A (10 x 2 = 20 Marks)
(Answer all Questions)

		CO	RBT LEVEL
1.	Convert (1,3215) to binary.	1	2
2.	List the characteristics of grey code.	1	2
3.	Draw the circuit of half subtractor.	2	2
4.	Define De- multiplexing.	2	2
5.	Draw the characteristic ' table of SR Latch.	3	2
6.	Compare Sequential and combinational circuit.	3	3
7.	What is the use of primitive flow table.	4	2
8.	What is a Cycle?	4	2
9.	List the different types of ROM.	5	2
10.	List the operations performed in a memory.	5	2

PART- B (5 x 14 = 70 Marks)

		Marks	CO	RBT LEVEL
11. (a)	Construct the given using only NOR gates F(a,b,c,d,) = Pi (1,3,4,5,7,9,11,13,14)	(14)	1	4

(OR)

1

(b) Simplify using K Map method   (14)   1   4

$F(A,B,C,D,E) = (0,2,5,7,9,11,15,17,18,20,24,25,30,31,) + d(1,4,10,13,14,,21,25)$

12. (a) Design a BCD to Excess3 code convertor.   (14)   2   3

(OR)

(b) Design a multiplexer circuit for the boolean function   (14)   2   3

$F(A,B,C,D) = (1,3,4,5,7,8,,11, 14,15)$

13. (a) Explain in detail about the various types of shift register.   (14)   3   4

(OR)

(b) With a neat diagram explain the working of a 4 bit ring counter.   (14)   3   4

14. (a) Discuss in detail about the various hazards that exists in a digital system.   (14)   4   3

(OR)

(b) Design a gated latch circuit with two inputs G (gate) and D (data), and one output Q. Binary information present at the D input is transferred to the Q output when G=1. The Q output will follow the D input as long as G=1. When G goes to 0, the information that was present at the D input at the time the transition occurred is retained at the Q output.   ()   4   3

15. (a) Discuss in detail about the various error detection and correcting codes.   (14)   5   3

(OR)

(b) Implement the following Boolean functions using PLA: (14)   5   3

$F1(A,B,C) = (01,2,4)$

PART- C (1 x 10 = 10 Marks)
(Q.No.16 is compulsory)

		Marks	CO	RBT LEVEL
16.	Design and implement a 3-bit synchronous counter.	(10)	2	5

****