Q. Code: 677809

Reg. No. | | | | | | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATION, MAY 2023

Fourth Semester

CS18401 – COMPUTER ARCHITECTURE

(Computer Science and Engineering)

(Regulation2018 / 2018A)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Understand Bus structure and Instruction set	**2**
CO 2	Design Arithmetic and Logic unit.	**3**
CO 3	Design of Control units.	**3**
CO 4	Understand Parallel processing	**2**
CO 5	Evaluate performance of Memory.	**5**

PART- A (10 x 2 = 20Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	What are the components of computer system?	**1**	**1**
2.	Write the basic performance equation.	**1**	**1**
3.	What is overflow in floating point arithmetic?	**2**	**1**
4.	Perform the addition of following numbers 1101,1001	**2**	**2**
5.	Define hazard. Give an example for control hazard.	**3**	**2**
6.	Brief about branch prediction buffer.	**3**	**2**
7.	Describe the main idea of Parallel processing architectures.	**4**	**2**
8.	Define multicore microprocessor.	**4**	**1**
9.	Define hit rate and miss rate.	**5**	**1**
10.	Differentiate paging and segmentation.	**5**	**2**

PART- B (5x 14=70Marks)

		Marks	CO	RBT LEVEL
11. (a)	Give appropriate examples to explain the various addressing modes and describe the application of each.	**(14)**	**1**	**3**
	(OR)			
(b)	Discuss the various instructions formats and illustrate with an example.	**(14)**	**1**	**3**

12. (a)	Multiply unsigned numbers 13 as Multiplicand and 11 as multiplier using booths algorithm to find the product.	**(14)**	**2**	**4**
	(OR)			
(b)	Divide (12_{10} / 3_{10}) using restoring division methods with necessary flowchart and steps. Find the quotient and remainder.	**(14)**	**2**	**4**
13. (a)	Explain in detail about types of pipeline hazards and how the performance degradation can be resolved in data hazards with an example?	**(14)**	**3**	**3**
	(OR)			
(b)	With an example, explain the impact of pipelining on instruction set design.	**(14)**	**3**	**3**
14. (a)	Compare and contrast Fine grained, Coarse grained multithreading and Simultaneous Multithreading.	**(14)**	**4**	**4**
	(OR)			
(b)	Identify the Flynn classification and give an example for each class in Flynn's classification.	**(14)**	**4**	**4**
15. (a)	Explain in detail about interrupts and What the CPU does with interruptions. Discuss thoroughly with a clean diagram.	**(14)**	**5**	**4**
	(OR)			
(b)	Direct Memory Access can improve I/O speed? Justify with necessary explanation and block diagram.	**(14)**	**5**	**4**

PART- C (1x 10=10Marks)

(Q.No.16 is compulsory)

		Marks	CO	RBT LEVEL
16.	Our favorite program runs in 10 seconds on computer A, which has a 2.2 GHz Clock. We are trying to help a computer designer build a computer, B, which will run this program in 8 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.5 times as many clock cycles as Computer A for this program. What clock rate should we tell the designer to target?	**(10)**	**1**	**5**