Q. Code:553716

Reg. No. | | | | | | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATIONS, MAY 2023

Third Semester

EC18304 – DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering)

(Regulation 2018A)

TIME: 3 HOURS **MAX. MARKS: 100**

CO 1 Analyze different methods used for simplification of Boolean expressions.
CO 2 Design various combinational circuits using logic gates.
CO 3 Analyze and design synchronous and asynchronous sequential circuits.
CO 4 Design a RAM, ROM, PAL and PLA devices.
CO 5 Write simple HDL codes for digital circuits.

PART- A (10x2=20Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Convert the $(256.48)_{10}$ in to its equivalent hexadecimal.	**1**	**3**
2.	Express the function Y = A+B´C in canonical POS.	**1**	**3**
3.	Implement AND gate using only NOR gates.	**2**	**3**
4.	What is priority encoder?	**2**	**1**
5.	Convert D flip-flop to T flip-flop.	**3**	**3**
6.	How many flip-flops are required to build a binary counter that counts from 0 to 512?	**3**	**3**
7.	Compare and contrast the features of Mealy and Moore machines.	**4**	**3**
8.	Distinguish between PAL and PLA.	**4**	**3**
9.	What is state diagram? Give an example.	**5**	**1**
10.	Write the Verilog code for a full adder.	**5**	**3**

PART- B (5x 14=70Marks)

			Marks	CO	RBT LEVEL
11. (a)	**(i)**	Minimize the following logic function using K-map and realize using NAND and NOR gates. F (A, B, C, D) = ∑m (1, 3, 5, 8, 9, 11, 15) + d (2,13)	**(10)**	**1**	**3**
	(ii)	Implement EXOR gate using only NAND gates.	**(4)**	**1**	**3**
		(OR)			
	(b)	Minimize the given switching function using Quine - McCluskey method. F (A, B, C, D) = ∑m (0, 1, 2, 3, 4, 6, 8, 10, 12, 14)	**(14)**	**1**	**3**

12. (a)	Design a BCD adder and explain its working with necessary block diagram.	**(14)**	**2**	**2**
	(OR)			
(b)	With neat diagram explain the working of Carry Look Ahead adder.	**(14)**	**2**	**2**
13. (a)	Design and implement a synchronous decade counter. Explain its working. Draw the timing diagram.	**(14)**	**3**	**4**
	(OR)			
(b)	Design a Moore type sequence detector to detect a serial input sequence of 101.	**(14)**	**3**	**4**
14. (a)	Write the differences between static and dynamic RAM. Draw the circuits of one cell of each and explain its working.	**(14)**	**4**	**4**
	(OR)			
(b)	Design using PAL the following Boolean functions. W (A, B, C, D) = ∑ (2, 12, 13) X (A, B, C, D) = ∑ (7, 8, 9, 10, 11, 12, 13, 14, 15) Y (A, B, C, D) = ∑ (0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15) Z (A, B, C, D) = ∑ (1, 2, 8, 12, 13)	**(14)**	**4**	**4**
15. (a)	Design an asynchronous sequential circuit that has 2 inputs x_1 and x_2 and one output z. When x_1 = 0, output is zero. The change in x_2 that occurs while x_1 is 1 will cause output z =1. The output z will remain 1 until x_1 returns to 0. Realize the circuit using D flip-flop.	**(14)**	**5**	**4**
	(OR)			
(b)	**(i)** Write a Verilog code for 3:8 decoder.	**(7)**	**5**	**4**
	(ii) Write a Verilog code for 8:1 Multiplexer.	**(7)**	**5**	**4**

PART- C (1x 10=10Marks)

(Q.No.16 is compulsory)

		Marks	CO	RBT LEVEL
16.	Construct a BCD to Excess-3 code convertor using minimum number of NAND gates.	**(10)**	**2**	**5**

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