

Reg. No.

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B.E. / B.TECH. DEGREE EXAMINATIONS, MAY 2023
 Fifth Semester
EC18503– COMPUTER ORGANIZATION AND DESIGN
(Electronics and Communication Engineering)
(Regulation 2018)

TIME: 3 HOURS**MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Compute the performance of various computer architecture and to interpret the instruction set of MIPS processor.	4
CO 2	Design and construct various arithmetic circuits for an Arithmetic and Logic units of computing systems.	4
CO 3	Assessing various pipelining techniques to implement it for better data-path construction for control units of computing systems.	3
CO 4	Categorize various paralleling process techniques and its challenges and also to distinguish various multithreading techniques.	3
CO 5	Organize the different memory technologies and I/O systems to be preferred for computer architectural design.	4

PART- A (10 x 2 = 20 Marks)

(Answer all Questions)

	CO	RBT LEVEL
1. Draw the structure of 'I' format of MIPS instructions and explain.	1	2
2. Define CPI.	1	1
3. Subtract $(11010)_2 - (10000)_2$ using 1's complement and 2's complement.	2	3
4. Justify the need for sub word parallelism in computing system.	2	3
5. What are the elements used to fetch instructions and increment the PC?	3	2
6. What is pipelining?	3	1
7. What are multicore processors?	4	1
8. State the challenges of parallel processing.	4	2
9. List the levels of memory hierarchy.	5	2
10. What is virtual memory?	5	1

PART- B (5 x 14 = 70 Marks)

	Marks	CO	RBT LEVEL
11. (a) What is an addressing mode in a computer? Describe the MIPS addressing modes with suitable examples to each category.	(14)	1	3

(OR)

(b) Illustrate the Eight great ideas with one example for each. (14) 1 3

12. (a) Explain in detail about floating point addition with example. (14) 2 3

(OR)

(b) Discuss in detail about non restoring division algorithm in detail with diagram and examples. (14) 2 3

13. (a) Design a simple data path with the control unit and explain the execution of R type instructions format. (14) 3 3

(OR)

(b) Describe the pipeline hazards and the various techniques used to overcome the hazards in detail. (14) 3 3

14. (a) Demonstrate the different classes of hardware multi-threading with necessary diagrams. (14) 4 3

(OR)

(b) Categorize the computers based on Flynn's classification with necessary diagrams. (14) 4 3

15. (a) Discuss the different mapping techniques used in cache memories and their relative merits and demerits. (14) 5 3

(OR)

(b) Discuss in detail the ways for improving cache performance. (14) 5 3

PART- C (1 x 10 = 10 Marks)

(Q.No.16 is compulsory)

Marks CO RBT
LEVEL

16. Solve the following using restoring division algorithm. (10) 2 5
Dividend(Q) = (12)₁₀ Divisor (M) = (4)₁₀.
