Q. Code: 349709

Reg. No. | | | | | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATIONS, MAY 2023

Sixth Semester

EC18601 – VLSI DESIGN

(Electronics and Communication Engineering)

(Regulation 2018)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Sketch the CMOS logic circuit using Stick Diagrams and Layout Diagrams.	**3**
CO 2	Identify the MOS circuits for various combinational logic blocks and analyze performance parameters.	**4**
CO 3	Develop Sequential logic blocks and perform timing analysis.	**4**
CO 4	Detect suitable MOS logic style for designing arithmetic logic blocks.	**3**
CO 5	Compute FPGA and perform testing.	**3**

PART- A (10 x 2 = 20 Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Compare enhancement MOS and depletion MOS.	**1**	**4**
2.	Compare Stick Diagram and Layout Diagram.	**1**	**4**
3.	Define Elmore's delay model.	**2**	**2**
4.	Write the expression and draw a 2x1 multiplexer using transmission gate logic.	**2**	**2**
5.	In a bistable circuit, how is the stable state changed from one to another?	**3**	**4**
6.	Why does clock gating reduce dynamic power?	**3**	**4**
7.	Analyze the pros and cons of Carry Select Adders.	**4**	**4**
8.	Draw the block diagram of a 4 bit adder using the inversion property.	**4**	**2**
9.	What are the various types of programming technologies used in FPGA design.	**5**	**2**
10.	Distinguish between 'Verification' and 'Testing' in IC design cycle.	**5**	**4**

PART- B (5 x 14 = 70 Marks)

			Marks	CO	RBT LEVEL
11. (a)		Apply the lambda (λ) and beta (β) scaling principles to various device parameters and discuss. Mention the limitations of scaling principles.	**(14)**	**1**	**3**
		(OR)			
(b)	**(i)**	Design CMOS logic circuit for $Y = \overline{AB(C+D)}$ and draw the stick diagram.	**(8)**	**1**	**3**
	(ii)	Draw the layout diagram for the above circuit and *mark* minimum of *six different design rules*.	**(6)**	**1**	**3**

12. (a)	For the given Boolean expression, draw the logic circuit using the logic family mentioned below and compare the features and limitations of these logic families $Y = \overline{A + BC}$ (5) a) Pseudo NMOS (3) b) Differential Cascode Voltage Switch Logic (DCVSL) (3) c) Domino Logic (3)	**(14)**	**2**	**4**
	(OR)			
(b)	Discuss about the arising of monotonicity woes in cascading the dynamic circuits and how it is overcome in the Domino logic circuits.	**(14)**	**2**	**4**
13. (a)	Draw and explain the operation of a Transmission Gate Mux based ***Positive*** Edge Triggered ***Static*** register and analyze the minimum clock period needed for reliable operation.	**(14)**	**3**	**4**
	(OR)			
(b)	In a pipelined data path using C2MOS latches, what are the constraints on the logic function blocks during 0-0 overlap and 1-1 overlap of the clock? Explain in detail with illustration.	**(14)**	**3**	**4**
14. (a)	Draw the Booth multiplier structure, the Booth-encoder and Booth selector blocks. Justify how Booth algorithm speeds up the multiplication process using suitable illustration of a (6 x 6) multiplication.	**(14)**	**4**	**4**
	(OR)			
(b)	**(i)** Draw an 8-bit Logarithmic Barrel Shifter and bring out the features of barrel shifters. Assuming the control bits to be 0 1 1, plot the trace from any one of the inputs to output path.	**(7)**	**4**	**4**
	(ii) With suitable diagrams, bring out the features of Wallace Tree multiplier.	**(7)**	**4**	**4**
15. (a)	Discuss in detail about Full custom design, Semi-custom design and Standard cell design.	**(14)**	**5**	**2**
	(OR)			
(b)	Discuss in detail about Ad-Hoc Testing, Scan based testing and Boundary scan testing.	**(14)**	**5**	**2**

PART- C (1 x 10 = 10 Marks)

(Q.No.16 is compulsory)

		Marks	**CO**	**RBT LEVEL**
16.	Discuss about the role of the intermediate functions P and G in speeding up the addition in any 2 types of adders.	**(10)**	4	**5**

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