

1	How do high-K dielectrics solve the problem of Gate leakage?	1	4
2	State Moore's law.	1	1
3	Write the Matthiessen's rule for conductivity.	2	2
4	What is Einstein relation in semiconductor?	2	2
5	Draw the energy band diagram of an ideal MOS capacitor at negative gate bias.	3	3
6	Mention some methods to control the threshold voltage in a MOS device.	3	2
7	Write the drain current equation of MOSFET in terms of channel length.	4	3
8	What is velocity saturation and what is its effect on the I–V relation of a	4	3
	MOSFET?		
9	List the advantages of SOI Devices.	5	3
10	What are the applications of FINFET?	5	2

## **PART- B (5 x 14 = 70 Marks)**

		Marks	CO	RBT
				LEVEL
11. (a)	What is the need for high-K dielectrics and discuss the parameters to be	(14)	1	3
	considered while choosing a suitable alternative material to SiO <sub>2</sub> .			

## (OR)

<b>(b)</b>	Describe in detail about the various short channel effects in MOS device.	(14)	1	3
12. (a)	Briefly discuss about the electron transport in quantum wells and quantum wires.	(14)	2	3
	(OR)			
<b>(b)</b>	Write in detail about the electron transport in semiconductors, drift and diffusion model and related their models.	(14)	2	3
13. (a)	Sketch the C–V characteristics of a MOS capacitor with an n-type substrate under the low-frequency condition. How do the characteristics change for the high-frequency condition?	(14)	3	4
	(OR)			
(b)	Analyze the effect of fixed oxides charges and interface trapped charges in the MOS capacitors.	(14)	3	4
14. (a)	Discuss the I–V characteristics of the MOSFET when biased in the non-saturation and saturation regions.	(14)	4	3
	(OR)			
(b)	Discuss in detail about the field dependent mobility and subthreshold current in MOSFET.	(14)	4	3
15. (a)	With neat diagrams, explain the construction and working of FINFET. <b>(OR)</b>	(14)	5	3
(b)	What is SOI devices? List and explain the different types of SOI devices.	(14)	5	3
	<u>PART- C (1 x 10 = 10 Marks)</u>			
	(Q.No.16 is compulsory)			
		Marks	CO	RBT LEVEL

16. Analyze the various issues faced due to the scaling down of MOSFET (10) 1 4 devices.

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