**Q. Code: 431905**

**Reg. No.** | | | | | | | | | | | | | | |

# B.E / B.TECH. DEGREE EXAMINATION, MAY 2023

Fourth Semester

## EE18402 – DIGITAL LOGIC CIRCUITS

*(Electrical and Electronics Engineering)*

**(Regulation 2018/ Regulation 2018A)**

**TIME: 3 HOURS** **MAX. MARKS: 100**

**CO1** Understand various aspects of Boolean algebra.

**CO2** Design and evaluation of combinational logic circuits.

**CO3** Design and evaluation of sequential logic circuits.

**CO4** Design and analysis of asynchronous sequential logic circuits through VHDL.

**CO5** Comprehend the operation and characteristics of memory devices and digital logic families.

### PART- A (10x2=20Marks)

(Answer all Questions)

| | | CO | RBT LEVEL |
|---|---|---|---|
| **1.** | Realize AND gate using NOR-NOR Logic. | **1** | **3** |
| **2.** | Convert $(375.46)_8$ to hexadecimal value. | **1** | **3** |
| **3.** | Express the function Y=A + B'C in canonical POS form. | **2** | **3** |
| **4.** | Draw the block diagram and truth table for 2 to 4 decoder. | **2** | **2** |
| **5.** | Differentiate combinational and sequential circuits based on memory. | **3** | **2** |
| **6.** | Give the characteristic equation and truth table of T flip-flop. | **3** | **2** |
| **7.** | What is meant by race condition in asynchronous sequential circuits and mention its types? | **4** | **2** |
| **8.** | Write the VHDL program for NOT gate using dataflow modeling. | **4** | **2** |
| **9.** | Mention the important characteristics of ICs. | **5** | **1** |
| **10.** | How the memories are classified? | **5** | **2** |

### PART- B (5x 14=70Marks)

| | | | Marks | CO | RBT LEVEL |
|---|---|---|---|---|---|
| **11. (a)** | | Plot the logical expression ABCD + AB'C'D' + AB'C + AB on a 4-variable K-map; obtain the simplified expression from the map. Also realize the same using NAND logic. | **(14)** | **1** | **3** |
| | | **(OR)** | | | |
| **(b)** | **(i)** | Explain in detail about the binary codes. | **(8)** | **1** | **2** |
| | **(ii)** | Apply Boolean laws to reduce the Boolean expression. (A+C) (AD +AD') + AC + C | **(6)** | **1** | **3** |

| | | | | | |
|---|---|---|---|---|---|
| **12. (a)** | | Design and implement a gray to binary code converter. | **(14)** | **2** | **3** |
| | | **(OR)** | | | |
| **(b)** | **(i)** | Implement a full adder with two 4 x 1 multiplexers. | **(7)** | **2** | **3** |
| | **(ii)** | Design a binary to octal decoder circuit and explain its working with truth table. | **(7)** | **2** | **3** |
| **13. (a)** | **(i)** | A sequential circuit with two D flip flops A and B; inputs X and Y; output Z is specified by the following next state and output equations<br>$A^+$=X'Y+XA (a) Draw the logic diagram of the circuit (3)<br>$B^+$=X'B+XA (b) Derive the state table (3)<br>Z=B (c) Derive the state diagram (2) | **(8)** | **3** | **3** |
| | **(ii)** | Design a synchronous MOD 5 counter using T flip flops. | **(6)** | **3** | **3** |
| | | **(OR)** | | | |
| **(b)** | | Explain in detail about any two types of shift registers with neat output waveforms. | **(14)** | **3** | **3** |
| **14. (a)** | | Design an asynchronous circuit that has two inputs $X_1$ and $X_2$ and one output Z. The circuit is required to give an output whenever the input sequence (0,0) (0,1) and (1,1) received but only in that order. Design it using T flip-flop. | **(14)** | **4** | **3** |
| | | **(OR)** | | | |
| **(b)** | **(i)** | Write the VHDL code for JK flip-flop using behavioral modeling. | **(7)** | **4** | **2** |
| | **(ii)** | Construct a hazard-free logic circuit for a boolean function $f(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 10, 12)$. | **(7)** | **4** | **3** |
| **15. (a)** | | Implement the following function using PLA.<br>$F1=\sum m (0,1,2,3,4,7,8,11,12,15)$<br>$F2=\sum m (2,3,6,7,8,9,12,13)$<br>$F3=\sum m (1,3,7,8,11,12,15)$<br>$F4=\sum m (0,1,4,8,11,12,15)$ | **(14)** | **5** | **3** |
| | | **(OR)** | | | |
| **(b)** | | Draw and explain the implementation of the universal gates using CMOS. | **(14)** | **5** | **3** |

## PART- C (1x 10=10Marks)

(Q.No.16 is compulsory)

| | | Marks | CO | RBT LEVEL |
|---|---|---|---|---|
| **16.** | Design a three bit ripple up counter using JK flip-flops with timing diagram for each flip flop output. | **(10)** | **3** | **3** |

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