Q. Code:996107

Reg. No. | | | | | | | | | | | | | | |

B. E / B. TECH.DEGREE EXAMINATION, MAY 2023

Seventh Semester

EE18702 – VLSI AND EMBEDDED SYSTEMS

(Electrical and Electronics Engineering)

(Regulation 2018)

TIME:3 HOURS **MAX. MARKS: 100**

CO1 Learn about the VLSI design process and its properties.
CO2 Acquire knowledge to design combinational circuits using MOS.
CO3 Acquire knowledge about embedded system and processors and their applications.
CO4 Learn about the networking protocols and its applications.
CO5 Understand the concepts of RTOS in embedded system.

PART- A(10x2=20Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Discuss the importance of W, L and D (oxide thickness) in a MOSFET design.	**1**	**2**
2.	Draw the structure of depletion mode in NMOS transistor.	**1**	**2**
3.	Design a 2 x1 multiplexer using transmission gate.	**2**	**3**
4.	Distinguish between dynamic CMOS logic and clocked CMOS logic.	**2**	**2**
5.	What are the characteristics of embedded computing applications?	**3**	**1**
6.	Compare Harvard and Von Nuemann architecture.	**3**	**3**
7.	List the features of RS232C.	**4**	**1**
8.	Define BAUD rate.	**4**	**1**
9.	What do you mean by process, task and thread?	**5**	**2**
10.	Define mutex semaphore.	**5**	**1**

PART- B (5x 14=70Marks)

				Marks	CO	RBT LEVEL
11. (a)	**(i)**	Explain the MOS transistor operation with the help of neat sketches in the Enhancement mode.		**(7)**	**1**	**2**
	(ii)	Discuss the different regions in CMOS inverter, current characteristics and derive the expression related to region 3.		**(7)**	**1**	**2**
		(OR)				
(b)	**(i)**	Discuss in detail the various steps involved in VLSI design flow.		**(7)**	**1**	**2**
	(ii)	Derive the expression for the threshold voltage of MOSFET.		**(7)**	**1**	**2**

12. (a)	**(i)**	Design an 8:1 MUX using transmission gates. Write its logical expression and also draw its schematic diagram.	**(7)**	**2**	**3**
	(ii)	Design a CMOS logic to implement the given expression Y= (A.(B+C) + D.E).	**(7)**	**2**	**3**
		(OR)			
(b)		Discuss in detail about the complementary pass-transistor logic (CPL) and implement a four input NAND gate..	**(14)**	**2**	**2**
13. (a)		Sketch the structural units in embedded processor and demonstrate their functions in detail.	**(14)**	**3**	**2**
		(OR)			
(b)	**(i)**	Demonstrate the working of DMA with help of a neat sketch.	**(7)**	**3**	**2**
	(ii)	Explain the use of monitor for target hardware debugging.	**(7)**	**3**	**2**
14. (a)		Sketch the I2C bus serial communication protocol and describe the same. Compare and comment on its performance with other serial communication protocols.	**(14)**	**4**	**2**
		(OR)			
(b)		Explain the RS232 serial communication standard in detail and compare it with other standards.	**(14)**	**4**	**2**
15. (a)		Discuss about multiple process and interprocess communication mechanisms.	**(14)**	**5**	**2**
		(OR)			
(b)		Discuss any two scheduling policies used in multiprocess environment.	**(14)**	**5**	**2**

PART- C (1x 10=10Marks)

(Q.No.16 is compulsory)

			Marks	CO	RBT LEVEL
16.		Mention the two rules of interrupt routines in an RTOS environment. With an example, briefly explain, what happens when each rule is violated.	**(10)**	**5**	**5**

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