Q. Code: 910481

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Reg. No. | | | | | | | | | | | | | |

B.E / B.TECH. DEGREE EXAMINATIONS, MAY 2023

Third Semester

IT18302 – COMPUTER ORGANIZATION AND ARCHITECTURE

(Information Technology)

(Regulation 2018A)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Build the basic structure of computer, operations and instructions	**3**
CO 2	Design Arithmetic and Logic Unit	**3**
CO 3	Discuss the pipelined execution and design control unit	**3**
CO 4	Evaluate performance of memory systems	**3**
CO 5	Construct the parallel processing architectures	**3**

PART- A (10 x 2 = 20 Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	List the types of instructions available in Basic computer.	**1**	**2**
2.	Differentiate direct addressing mode and indirect addressing mode with an example.	**1**	**3**
3.	Solve 2*3 using Booth multiplication algorithm.	**2**	**3**
4.	Solve (5*8)+(3-2) using Reverse Polish notation.	**2**	**3**
5.	List the five elements of Datapath.	**3**	**2**
6.	Draw the datapath for loading the next instruction in program counter.	**3**	**3**
7.	Write the formula for write stall cycles.	**4**	**2**
8.	Differentiate between programmed I/O and Interrupts.	**4**	**3**
9.	Differentiate between uniform memory access and non-uniform memory access.	**5**	**3**
10.	Differentiate between single core processors and multicore processors.	**5**	**3**

PART- B (5 x 14 = 70 Marks)

		Marks	CO	RBT LEVEL
11. (a)	Draw a flowchart for Instruction cycle and Interrupt cycle (complete Computer description) with a neat diagram.	**(14)**	**1**	**3**
	(OR)			
(b)	Design an accumulator unit of a basic computer.	**(14)**	**1**	**3**

12. (a)	Draw the flowchart for division algorithm using restore method and solve 7%5 using restore method.	**(14)**	**2**	**3**
	(OR)			
(b)	Examine in detail various instruction format available in basic computer with an example.	**(14)**	**2**	**3**
13. (a)	Draw and examine data path for R type instruction, load, store and branch instruction along with the control signals.	**(14)**	**3**	**3**
	(OR)			
(b)	Examine in detail about the concept of pipeline architecture, various hazards in pipeline architecture and techniques to overcome the hazards in pipeline architecture.	**(14)**	**3**	**3**
14. (a)	Discuss in detail the working of cache memory, various types of cache memories available and measuring performance in cache memory with a neat diagram.	**(14)**	**4**	**2**
	(OR)			
(b)	Discuss in detail, how data is transferred through Direct memory access and also explain various bus arbitration schemes available in DMA with a neat diagram.	**(14)**	**4**	**2**
15. (a)	Examine in detail various types of Flynn classification with an example.	**(14)**	**5**	**3**
	(OR)			
(b)	Examine in detail the concept of hardware multithreading and its types with an example.	**(14)**	**5**	**3**

PART- C (1 x 10 = 10 Marks)

(Q.No.16 is compulsory)

		Marks	CO	RBT LEVEL
16.	Design a basic computer with a neat diagram.	**(10)**	1	**5**

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