B.E./B.TECH. Degree Examination, December 2020

Third Semester

CS18303 – Microprocessor and its Applications

(Regulation 2018)

Time: Three hours Maximum : 80 Marks

Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. Consider the following statements.

   I. Daisy chaining is used to assign priorities in attending interrupts.

   II. When a device raises a vectored interrupt, the CPU does polling to identify the source of the interrupt.

   III. In polling, the CPU periodically checks the status bits to know if any device needs its attention.

   IV. During DMA, both the CPU and DMA controller can be bus masters at the same time

   Which of the above statements is/are TRUE?

   A. III only

   B. I and IV only

   C. I and III only

   D. I and II only

2. Which of the following 8251 signal is not used to control MODEM?

   A. TxRDY

   B. DSR

   C. DTR

   D. CTS

3. In power down mode of power control register which of the following is not true?

   A. All functions are stopped, the contents of the on-chip RAM and Special Function Registers are lost

   B. The ALE and PSEN output are held low

   C. Last instruction executed before going into the power down mode

   D. The on-chip oscillator is stopped

4. Which pins of an 8051 microcontroller function as the RxD and TxD pins during a serial communication operation?

   A. TxD – P3.1, RxD – P3.0

   B. TxD – P3.0, RxD – P3.1

   C. TxD – P3.0, RxD – P3.0

   D. TxD – P3.1, RxD – P3.1

5. How is a macro different from a procedure?
6. Differentiate maskable and non-maskable interrupts? How will you mask an interrupt in 8086?
7. What is the difference between Mode 0, Mode 1 and Mode 2 operations of 8255?
8. How do you select the register bank in 8051 micro-controllers?

PART B - (4 X16 = 64 marks)

09. (a) With a neat architectural diagram of 8086, explain the register structure and advantage of pipelining feature in 8086 architecture. **(16)**

(OR)

(b) (i) Illustrate with suitable examples about the memory addressing modes in 8086 microprocessor. **(8)**

(ii) Analyze the working of following assembler directives: END P, EQU, EVEN, EXTRN with examples. **(8)**

10. (a) (i) Compare the schemes used to solve the bus arbitration problem in multiprocessor configurations. **(8)**

(ii) Differentiate between memory mapped I/O and I/O mapped I/O. **(8)**

(OR)

(b) Explain how the Intel Pentium processor's supports pipelining and superscalar techniques. **(16)**

11. (a) With suitable diagram, explain how the Priority Interrupt Controller 8259 can be interfaced with 8086 in cascade mode. **(16)**

(OR)

(b) How to interface the Hex Key pad and 7- segment LEDs using 8279 with 8086 microprocessor. Illustrate with suitable diagram supported for it. **(16)**

12. (a) How can you explain the architecture of 8051 microcontroller instead of microprocessor. **(16)**

(OR)

(b) With the help of IoT compenents design your own IoT architecture. Comment on your design. **(16)**