B.E./B.TECH. Degree Examination, December 2020

Third Semester

EC18304 – Digital System Design

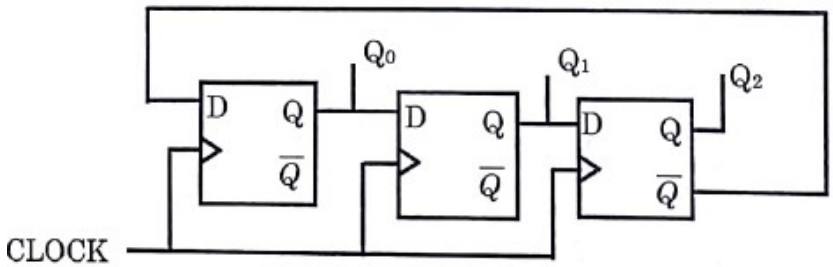
(Regulation 2018)

Time: Three hours Maximum : 80 Marks

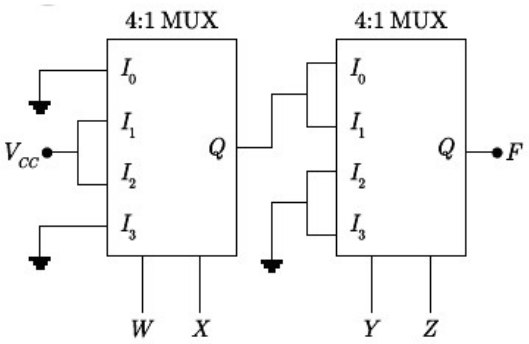
Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. A bulb in a staircase has two switches, one switch being at the ground floor and another at the first floor. The bulb can be turned ON by anyone of the switches irrespective of the state of another one. The logic of switching of the bulb resembles
   (a) OR gate (b) AND gate (c) NOT gate (d) XOR gate
2. The output Y of a 2-bit comparator is at logic 1 whenever input A is greater than input B. The no. of combinations for which the output is at logic 1 are
   (a) 4 (b) 6 (c) 16 (d) 8
3. What is the output ($Q_0Q_1Q_2$) of the register formed from D flip flops at the end of 4 clock cycles? Let the initial output be 000.



   (a) 110 (b) 000 (c) 011 (d) 001
4. How many flip-flops are requied to construct a decade counter?
   (a) 4 (b) 8 (c) 5 (d)10
5. A function of Boolean Variables X, Y and Z is expressed in terms of the min-terms as F (X, Y, Z) = ∑ m (**1, 2, 5, 6, 7**). What is the simplified Boolean expression of the given function in canonical product of sums (POS) form?
6. In the given logical diagram, W and Y are the MSBs of selection inputs. Find an expression for the output F.



7. A 3 to 8 decoder can be used for binary to octal decoding. Which output line is activated when the input is 101_2? Draw the truth table of the decoder.
8. Differentiate static-0 and static-1 hazards.

PART B - (4 X16 = 64 marks)

09. (a) Using Quine-McCluskey method simplify the Boolean function **(16)**
F(A,B,C,D) = Σ m(0,1,2,3,5,7,8,10,12,13,15)

(OR)

(b) Design a combinational circuit that accepts a four bit binary coded decimal input and generates a four bit output which is 3 more than its input. Draw the truth table and logic diagram of the same. **(16)**

10. (a) Suggest a 4-bit binary adder which reduces the ripple carry delay and draw the logic diagram. **(16)**

(OR)

(b) (i) Implement the function F (A,B,C) = Σ (**1, 3, 5, 6**) using multiplexer. **(8)**

(ii) Design a 3-bit odd parity generator. **(8)**

11. (a) (i) Show how JK flip flop can be operated as T flip flop? Realize and draw the logic diagram. **(10)**

(ii) Construct a 4-bit register using D flip flop where a single bit '1' is made to circulate around it upon the application of clock pulses. **(6)**

(OR)

(b) Design a mod-8 synchronous counter using T flip flop. **(16)**

12. (a) Design the following Boolean functions using PAL. **(16)**
W (A, B, C, D) = ∑ (**2, 12, 13**)
X (A, B, C, D) = ∑ (**7, 8, 9, 10, 11, 12, 13, 14, 15**)
Y (A, B, C, D) = ∑ (**0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15**)
Z (A, B, C, D) = ∑ (**1, 2, 8, 12, 13**)

(OR)

(b) (i) Obtain a static hazard free circuit for the following switching function **(10)**
F (W,X,Y,Z) = Σ (**0,2,4,5,8,10,14**)

(ii) Write a Verilog HDL code to implement a full adder. **(6)**