B.E./B.TECH Degree Examination, December 2020

Fifth Semester

EC18503-Computer Organization and Design

(Regulation 2018)

Time: Three hours Maximum : 80 Marks

Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. The number $(1110.101001)_2$ in hexadecimal notation is
   (a)E.A4 (b)C.A4 (c) E.29 (d) C.29
2. In MIPS instruction BLT $S1,$S2,Label means:
   (a)If $S1 is less than $S2 then do not branch to location Label
   (b) If $S1 is less than $S2 then branch to location Label
   (c) If $S2 is less than $S1 then branch to location Label
   (d) If $S1 is not less $S2 then branch to location Label
3. In a vector processor, suppose that the start-up time of vector multiply operation is 25 clock cycles. After start-up, the initiation rate is five clock cycles. The number of clock cycles to process a 50-element vector will be (a) 200 (b) 250 (c) 275 (d) 25
4. Which of the following is true for a memory hierarchy?
   a. It tries to bridge the processor-memory speed gap.
   b. The speed of the memory level closest to the processor has the highest speed.
   c. The capacity of the memory level farthest away from the processor is the largest.
   d. It is based on the principle of locality of reference
   (a) a (b) b and c (c) a and c (d) All of the above
5. Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much?
6. Consider an instruction pipeline with three stages and the stage delays are 20 nsec, 18 nsec,12 nsec respectively. The inter stage register stage delay of the Pipeline is 4 nsec. Compare the speed up of the processor with Pipelined and non- pipelined implementation ,for the execution of 500 instructions.
7. Compare strong scaling with weak scaling.
8. Consider a direct mapped cache of size 32 KB with Block size 256 bytes. The size of main memory is 128 KB. Find the Number of Tag bits, Line number and Block offset.

PART B - (4 X16 = 64 marks)

09. (a) (i) Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2 **(5)**

Which processor has the highest performance expressed in instructions per second?

(ii) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions. **(5)**

(iii) If attempted to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction? **(6)**

(OR)

(b) (i) Assume variable **h** is associated with register **$s2** and the base address of the array **A** is in **$s3**. What is the MIPS assembly code for the C assignment statement **A[12] = h + A[8];** Also represent all the MIPS code in machine readable format. **(10)**

(ii) In the following code segment, f,g,h,i and j are variables which corresponds to MIPS registers $s0 to $s4, Write the equivalent MIPS code and elaborate on it. (6) **(6)**

```
if (i= =j)
f= g + h;
  Else
f= g - h;
```

10. (a) (i) Perform Multiplication operation using Booth's Algorithm for the given Signed Numbers Multiplicand = $(-12)_{10}$ Multiplier =$(7)_{10}$ **(8)**

(ii) Divide the following numbers using Restoration division technique Dividend(Q) =$(9)_{10}$ Divisor (M)= $(3)_{10}$ **(8)**

(OR)

(b) (i) Add the numbers $\mathbf{0.5_{10}}$ and $\mathbf{0.125_{10}}$ in binary using floating point addition Algorithm. Add suitable comments to each step along with its flowchart**.** **(8)**

(ii) Discuss in detail the floating point Multiplication Algorithm with its flowchart. **(8)**

11. (a) Design a simple data path with the control unit for an R-type instruction. **(16)**

(OR)

(b) (i) Explain the hazards caused in an instruction Pipeline. **(8)**

(ii) Describe Operand forwarding in a Pipeline processor with a diagram. **(8)**

12. (a) (i) Discuss the challenges in parallel Processing in enhancing Computer Architecture. **(12)**

(ii) Consider a fully associative cache with 8 cache blocks (0-7). The memory block requests are in the order- **(4)**

4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7

If LRU replacement policy is used, which cache block will have memory block 7? Calculate the hit ratio and miss ratio.

(OR)

(b) Discuss in detail the various methods for improving cache performance. **(16)**