Q. Code: 911267

B.E/B.TECH. Information Technology December 2020

Third Semester

IT18302-Computer Organization and Architecture

(Regulation 2018)

Time: Three hours Maximum : 80 Marks

Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. The addressing mode which makes use of in-direction pointers is _____
   a) Indirect addressing mode
   b) Index addressing mode
   c) Relative addressing mode
   d) Offset addressing mode
2. The addressing mode/s, which uses the PC instead of a general purpose register is _____
   a) Indexed with offset
   b) Relative
   c) Direct
   d) Both Indexed with offset and direct
3. The pipelining process is also called as _____
   a) Superscalar operation
   b) Assembly line operation
   c) Von Neumann cycle
   d) None of the mentioned
4. The interrupt-request line is a part of the _____
   a) Data line
   b) Control line
   c) Address line
   d) None of the mentioned
5. Explain briefly the difference between hardwired control and microprogrammed control with a real time example
6. Write a program (A+B)*(C+D) using one address format
7. Draw the datapath for instruction fetch cycle.
8. Differentiate GPU and normal cpu with a real time example.

PART B - (4 X16 = 64 marks)

09. (a) Draw and Explain the flowchart for Instruction cycle and Interrupt cycle (complete Computer description) with a neat diagram. **(16)**

(OR)

(b) Design and develop an accumulator logic with a neat diagram. **(16)**

10. (a) Draw the flowchart for division algorithm using restore method and solve 6%5 using restore method. **(16)**

(OR)

(b) Explain in detail working of stack in the basic computer and write the algorithm for push and pop operation in stack and solve (4+3)*(5+8) using reverse polish notation. **(16)**

11. (a) Draw and explain in detail data path for R type instruction, load, store and branch instruction along with the control signals. **(16)**

(OR)

(b) Explain in detail about the concept of pipeline architecture with a real time example, various hazards in pipeline architecture and techniques to overcome the hazards in pipeline architecture. **(16)**

12. (a) Explain in detail about cache memory, how is the element found in cache, types of cache and ways to improve cache performance. **(16)**

(OR)

(b) Explain how DMA is used for direct transfer of data between memory and peripherals and differentiate between DMA and programmed IO. **(16)**