B.E./B.TECH. Degree Examination, January 2021

Semester - III

EC18304 – Digital System Design

(Regulation 2018)

Time: Three hours Maximum : 80 Marks

Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. The boolean function F(A, B,C,D)=∑ m (1, 3, 7,11,15)+∑ d (0, 2, 5)

   (a)AB+C'D' (b)AB+CD' c)CD+A'B' (D)A'B+C'D

2. The number of select lines used for 32 to 1 Multiplexer is

   (a)4 (b)5 c)16 (d)6

3. The output of SR flipflop when S=1 and R=0

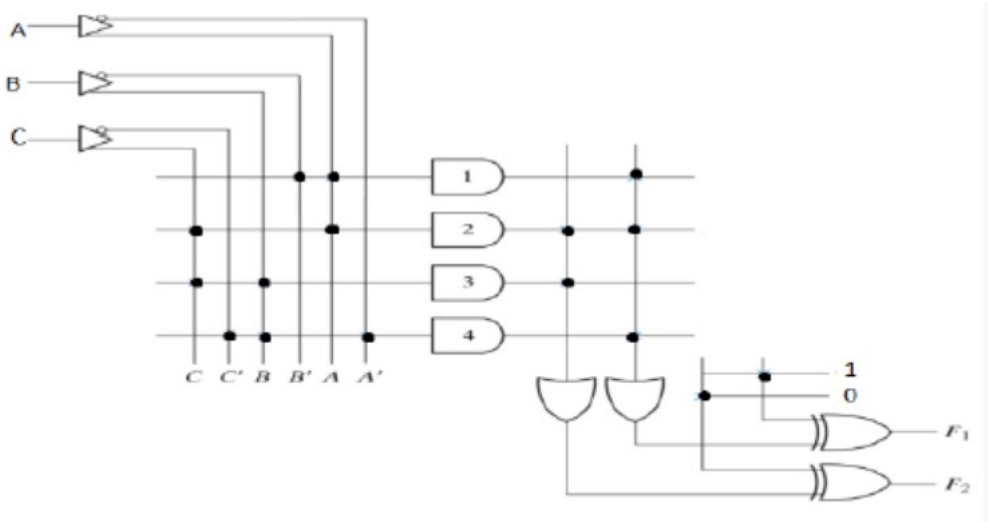
   (a) 1 (b) 0 (c) No change (d) High impedance

4. How many D flip-flops are required to construct MOD-8 Johnson ring counter?

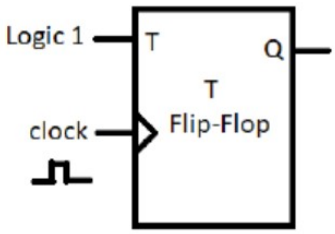
   (a) 6 (b)4 (c)3 (d)8

5. A function of Boolean Variables X, Y and Z is expressed in terms of the min-terms as F (X, Y, Z) = ∑ m (**1, 2, 5, 6, 7**). What is the simplified Boolean expression of the given function in canonical SOP form?

6. Give the Boolean expression for the functions F1 and F2 of the following PLA circuit.



7. What is the output frequency for 5 MHz clock signal?



8. Contrast static-0 and static-1 hazards.

PART B - (4 X16 = 64 marks)

09. (a) Find the minimal SOP for the Boolean expression using Tabulation method. **(16)**
$Y(A,B,C,D) = \Sigma\, m(1,2,3,7,8,9,10,11,14,15)$

(OR)

(b) Obtain minimal SOP for the function using 5-variable K-map **(16)**
$Y(V,W,X,Y,Z)=\Sigma\, m(1, 5,7,13,14,15,17,18,21,22,25,29)+\Sigma d\,(6,9,19,23,30)$

10. (a) Suggest a 4-bit binary coded Decimal adder which adds $(9)_{10}$ and $(5)_{10}$. Draw its truth table and logic diagram. **(16)**

(OR)

(b) (i) Implement the function $F(A,B,C)= \Sigma\, m(\mathbf{1, 2,3, 5,6,7})$ using 4 x 1 multiplexer. **(8)**

(ii) Design a 2-bit Magnitude comparator. **(8)**

11. (a) (i) Show how SR flip flop can be operated as JK flip flop? Realize and draw the logic diagram. **(10)**

(ii) Construct a 4-bit SISO register using D flip flop **(6)**

(OR)

(b) Design a BCD Synchronous counter using JK flip flop. **(16)**

12. (a) Design a 3-bit BCD to gray code converter using PLA. **(16)**

(OR)

(b) (i) Obtain a static hazard free circuit for the following switching function **(10)**
$F(A,B,C,D) = \Sigma\, (0,2,6,7,8,10,12)$

(ii) Write a Verilog HDL code to implement a 4X1 Demultiplexer. **(6)**