B.E./B.TECH. Degree Examination, January 2021

Semester – III

IT18302-Computer Organization and Architecture

(Regulation 2018)

Time: Three hours Maximum: 80 Marks

Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. A group of bits that tell the computer to perform a specific operation is known as____.
   a.Instruction code b.Micro-operation c.Accumulator d.Register
2. How to you represent the control function for condition if(P==1) then (R2<-R1)
   a)P:R2<-R1 b)P:R1<-R2 c)P;R2<-R1 d)P<-R2<-R1
3. For R-type instruction in the MIPS architecture ALU Op is
   a)1 b)10 c)110 d)101
4. Block address %(no of set in cache) is
   a)Direct mapped cache b)Set associative Cache c)Fully associative Cache
5. Differentiate microoperation from macrooperation.
6. Draw the format for double precision for IEEE 754 standard?
7. What is the formula to calculate memory stall cycle?
8. How do you differentiate uniform memory access from non-uniform memory access?

PART B - (4 X16 = 64 marks)

09. (a) (i) The following register transfers are to be executed in the system. For each transfer, specify. **(8)**
    i)the binary value that must be applied to bus
    select inputs S2,S1 and S0:
    ii)the register whose LD control input must be active.
    iii)a memory read or write operation.
    iv)the operation in the adder and logic circuit.

    (ii) Draw the timing sequence for the following instruction D_4T_4:SC=0 **(8)**

(OR)

(b) Draw the flow chart for Instruction cycle and interrupt cycle, also list the complete instruction set with timing cycles. **(16)**

10. (a) Draw the flowchart and solve 4/2 by non-restoring method algorithm. **(16)**

(OR)

(b) (i) Draw the flowchart and solve 3 X 2 by multiplication version 3 algorithm. **(10)**

(ii) Specify the control word that must be applied to the processor to implement the following micro operations. **(6)**

a)R1<-R2+R3

b)R4<-R4

c)R5<-R5-1

d)R6<-shl R1

e)R7<-input

11. (a) How to classify R-Type, I-type and J-type instruction? **(16)**

(OR)

(b) In a volfort computer, multiple instructions are trying to access the same resource. At a time only one instruction can access the resource. How do you define and overcome this conflict? Compare data unavailable problem and branch control problem in pipeline. **(16)**

12. (a) In what are all the ways you can map the content in memory with cache? And also state how do you measure and improve cache performance? **(16)**

(OR)

(b) How to classify programmed i/o, interrupt driven i/o and DMA? **(16)**