Q. Code: 487563

Reg. No. | | | | | | | | | | | | | |

B.E. / B.TECH. DEGREE EXAMINATIONS, MAY 2023

Second Semester

CS22202 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Computer Science and Engineering)

(Regulation 2022)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Students will be able to learn the different types of number systems and simplification of Boolean functions	**4**
CO 2	Students will be able to understand various logic gates and their usage	**2**
CO 3	Students will be able to study, analyze and design various combinational circuits and its implementation using VHDL	**4**
CO 4	Students will be able to understand the different type of memory and their structures	**2**
CO 5	Students will be able to study, analyze of RTL notation register operations in a clocked sequential circuit	**4**

PART- A (20 x 2 = 40 Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	Write the classification of binary codes.	**1**	**2**
2.	Represent a OR gate using NAND gate.	**1**	**3**
3.	What is the use of Don't care conditions?	**1**	**2**
4.	What is propagation delay?	**1**	**2**
5.	Draw 1:8 demultiplexer using two 1:4 Demultiplexer.	**2**	**3**
6.	What is magnitude comparator?	**2**	**1**
7.	How full adder is obtained from two half adders?	**2**	**3**
8.	Draw the circuit for 2-to-1 multiplexer.	**2**	**2**
9.	State the difference between latches and flipflops.	**3**	**2**
10.	Write any two applications of shift register.	**3**	**2**
11.	What is meant by edge triggered flip flops?	**3**	**2**
12.	Draw the excitation table of JK- flip flop.	**3**	**2**
13.	What are error detecting codes? Give examples.	**4**	**2**
14.	Draw the basic configuration of PROM.	**4**	**2**
15.	How many check bits are required for single bit error detection and correction?	**4**	**3**
16.	State the difference EPROM and EEPROM.	**4**	**2**
17.	List any two HDL operators and their symbols used in RTL design.	**5**	**2**
18.	Write a short note on register transfer level.	**5**	**2**
19.	Draw a block diagram for Sequential Binary Multiplier.	**5**	**2**
20.	Differentiate LOGICAL AND and BITWISE AND operators.	**5**	**2**

PART- B (5 x 10 = 50 Marks)

			Marks	CO	RBT LEVEL
21. (a)	**(i)**	Simplify the following Boolean expression to a minimum number of literals. A′B′ + A′C′D′ + A′B′D + A′B′CD′.	**(5)**	**1**	**4**
	(ii)	Convert the given expression in canonical SOP form Y = AC+AB+BC.	**(5)**	**1**	**4**
		(OR)			
(b)		State and Prove the Demorgan′s theorem and Consensus theorem.	**(10)**	**1**	**4**
22. (a)		Design a combinational circuit to convert binary to gray code.	**(10)**	**2**	**3**
		(OR)			
(b)		With neat diagram explain the 4-bit adder with carry look ahead.	**(10)**	**2**	**3**
23. (a)		With logic sketch explain the universal shift register as a storage device.	**(10)**	**3**	**3**
		(OR)			
(b)		Implement JK flip flop using D flip flop.	**(10)**	**3**	**3**
24. (a)		Explain in detail about the Programmable Logic Array, Programmable Programmable Logic.	**(10)**	**4**	**4**
		(OR)			
(b)		Explain about error detection and correction using hamming codes.	**(10)**	**4**	**2**
25. (a)		Explain in detail about the Algorithmic State Machine chart.	**(10)**	**5**	**2**
		(OR)			
(b)		Explain how a hardware description language includes operators that correspond to the register transfer operations of a digital system?	**(10)**	**5**	**4**

PART- C (1 x 10 = 10 Marks)

(Q.No.26 is compulsory)

		Marks	CO	RBT LEVEL
26.	Design a full subtractor and derive expression for difference and borrow. Realize the circuit using gates.	**(10)**	**2**	**5**

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