Q. Code: 767815

Reg. No. | | | | | | | | | | | | | |

B.E./ B.TECH. DEGREE EXAMINATIONS, MAY 2023

Second Semester

IT22201– COMPUTER ORGANIZATION AND ARCHITECTURE

(Information Technology)

(Regulation 2022)

TIME: 3 HOURS **MAX. MARKS: 100**

COURSE OUTCOMES	STATEMENT	RBT LEVEL
CO 1	Build the basic structure of computer, operations and instructions.	**4**
CO 2	Design arithmetic and logic unit.	**5**
CO 3	Design and analyze pipelined control units.	**5**
CO 4	Evaluate performance of memory systems.	**5**
CO 5	Construct the parallel processing architectures.	**5**

PART- A (20x2=40Marks)

(Answer all Questions)

		CO	RBT LEVEL
1.	What is the role of MAR and MDR?	**1**	**2**
2.	When you will say the instructions in the instruction set is complete?	**1**	**4**
3.	What do you understand from word length?	**1**	**2**
4.	What is an opcode? How many bits are needed to specify 32 distinct operations?	**1**	**2**
5.	How can we speed up the multiplication process?	**2**	**4**
6.	Solve 0.5_{10} + (-0.4375_{10}).	**2**	**3**
7.	Differentiate Register Stack and Memory stack.	**2**	**4**
8.	In floating point numbers when so you say that an underflow or overflow has occurred?	**2**	**2**
9.	How do control instructions like branch, cause problems in a pipelined processor?	**3**	**2**
10.	How addressing modes affect the instruction pipelining?	**3**	**4**
11.	Define Exceptions and Interrupts.	**3**	**2**
12.	What is the speedup of an ideal instruction pipeline?	**3**	**2**
13.	How many total bits are required for a direct-mapped cache with 16 KB of data and 4-word blocks, assuming a 32-bit address?	**4**	**3**
14.	Define locality in time and space.	**4**	**2**
15.	Why IO devices cannot be directly be connected to the system bus?	**4**	**4**
16.	Distinguish between memory mapped I/O and I/O mapped I/O.	**4**	**4**
17.	What is Symmetric Shared Memory?	**5**	**2**

18.	Differentiate process level parallelism and task level parallelism.	**5**	**4**
19.	Differentiate multi-core and multiprocessor.	**5**	**4**
20.	What are the different shared-memory multiprocessor models?	**5**	**2**

PART- B (5x 10=50Marks)

		Marks	CO	RBT LEVEL
21. (a)	Construct a bus system using registers, memory unit, load, Clear and increment signal and explain in detail.	**(10)**	**1**	**3**
	(OR)			
(b)	Examine the design of basic computer in detail.	**(10)**	**1**	**3**
22. (a)	Multiply 100111 with 11011 using Booth's algorithm.	**(10)**	**2**	**3**
	(OR)			
(b)	Explain how the expression X=A X B + C X C will be executed in one address, two address and three address processors in an accumulator organization.	**(10)**	**2**	**3**
23. (a)	Explain the need for pipelining? How we overcome the various types of Hazards?	**(10)**	**3**	**4**
	(OR)			
(b)	Analyze the data path construction with all the necessary functional units and control lines for an R-type instruction.	**(10)**	**3**	**4**
24. (a)	Explain how address translation is performed in virtual memory system and the role played by TLB to make the translation fast.	**(10)**	**4**	**2**
	(OR)			
(b)	Explain in detail about different types of Input Output module.	**(10)**	**4**	**2**
25. (a)	Infer the operation of centralized shared memory multiprocessor system with a neat diagram.	**(10)**	**5**	**4**
	(OR)			
(b)	Analyze FLYNN'S classification and multiprocessor benchmark in detail.	**(10)**	**5**	**4**

PART- C(1x 10=10Marks)

(Q.No.26 is compulsory)

		Marks	CO	RBT LEVEL
26.	Justify the advantage of restoring division by Performing the Division 11/3.	**(10)**	**2**	**5**