SRI VENKATESWARA COLLEGE OF ENGINEERING
(An Autonomous Institution, Affiliated to Anna University, Chennai)
SRIPERUMBUDUR TK.- 602 117
REGULATIONS – 2016
M.E. APPLIED ELECTRONICS
CURRICULUM AND SYLLABUS

SEMESTER I

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
1	MA16181	Applied Mathematics for Electronics Engineers	3	1	0	4
2	CU16103	Advanced Digital Signal Processing	3	1	0	4
3	AL16101	Advanced Digital Logic System Design	3	0	0	3
4	AL16102	Advanced Microprocessor and Microcontroller	3	0	0	3
5		Elective I	3	0	0	3
6		Elective II	3	0	0	3
PRACTICALS						
7	AL16111	Electronics System Design Laboratory I	0	0	3	2
		TOTAL	**18**	**2**	**3**	**22**

SEMESTER II

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
1	AL16201	Analysis and Design of Analog Integrated Circuits	3	0	0	3
2	AL16202	ASIC and FPGA Design	3	0	0	3
3	AL16203	Embedded Systems	3	0	0	3
4	CP16103	Multicore Architectures	3	0	0	3
5		Elective III	3	0	0	3
6		Elective IV	3	0	0	3
PRACTICALS						
7	AL16211	Electronics System Design Laboratory II	0	0	3	2
		TOTAL	**18**	**0**	**3**	**20**

SEMESTER III

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
1		Elective V	3	0	0	3
2		Elective VI	3	0	0	3
3		Elective VII	3	0	0	3
PRACTICALS						
4	AL16311	Project Work (Phase I)	0	0	12	6
		TOTAL	**9**	**0**	**12**	**15**

SEMESTER IV

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
PRACTICALS						
1	AL16411	Project Work (Phase II)	0	0	24	12
		TOTAL	**0**	**0**	**24**	**12**

TOTAL CREDITS TO BE EARNED FOR THE AWARD OF THE DEGREE: 69

M.E APPLIED ELECTRONICS.

ELECTIVE I

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
1	CU16005	Advanced Digital Image Processing	3	0	0	3
2	CU16007	Wavelet Transforms and Applications	3	0	0	3
3	CP16036	Soft Computing	3	0	0	3
4	AL16001	Computer Architecture and Parallel Processing	3	0	0	3
5	AL16002	Three Dimensional Network on Chip	3	0	0	3

ELECTIVE II

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
1	AL16003	CAD for VLSI Circuits	3	0	0	3
2	AL16004	Digital Control Engineering	3	0	0	3
3	AL16005	Hardware - Software Co Design	3	0	0	3
4	AL16006	Quantum Electronics	3	0	0	3
5	AL16007	Sensors and Signal Conditioning	3	0	0	3

ELECTIVE III

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
1	AL16008	VLSI Design Techniques	3	0	0	3
2	AL16009	Low Power VLSI Design	3	0	0	3
3	AL16010	Fiber Optic Sensors	3	0	0	3
4	AL16011	DSP Integrated Circuits	3	0	0	3
5	CU16016	RF System Design	3	0	0	3
6	AL16012	Analog and Mixed Mode VLSI Design	3	0	0	3

ELECTIVE IV

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
1	AL16013	Analog VLSI Design	3	0	0	3
2	AL16014	Physical Design of VLSI Circuits	3	0	0	3
3	AL16015	VLSI Signal Processing	3	0	0	3
4	AL16016	Data Converters	3	0	0	3
5	AL16017	Solid State Device Modeling and Simulation	3	0	0	3
6	NW16015	High Performance Networks	3	0	0	3

ELECTIVE V

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
1	AL16018	Testing of VLSI Circuits	3	0	0	3
2	AL16019	VLSI for Wireless Communication	3	0	0	3
3	AL16020	Photonics	3	0	0	3
4	AL16021	Nano Electronics	3	0	0	3
5	AL16022	Pattern Recognition	3	0	0	3
6	CU16017	Optical Computing	3	0	0	3

ELECTIVE VI

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
1	AL16026	Robotics	3	0	0	3
2	CU16018	Optical Imaging Techniques	3	0	0	3
3	AL16023	MEMS and NEMS	3	0	0	3
4	CU16004	Speech and Audio Signal Processing	3	0	0	3
5	AL16024	System on Chip Design	3	0	0	3
6	CP16035	Reconfigurable Computing	3	0	0	3
7	NW16016	Wireless Adhoc and Senor Networks	3	0	0	3

ELECTIVE VII

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
1	CU16203	Electromagnetic Interference and Compatibility	3	0	0	3
2	AL16027	Reconfigurable Architecture	3	0	0	3
3	AL16028	Multiprocessor Interconnection Network	3	0	0	3
4	AL16029	Mixed Signal VLSI Design	3	0	0	3
5	NW16022	Wireless Security	3	0	0	3

MA16181 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS

L	T	P	C
3	1	0	4

OBJECTIVES:

- The purpose of this course is to provide in-depth treatment on methods and techniques in Discrete-time signal transforms, digital filter design, optimal filtering, Power spectrum estimation, multi-rate digital signal processing.
- DSP architectures which are of importance in the areas of signal processing, control and communications.

UNIT I FUZZY LOGIC **9+3**

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers

UNIT II MATRIX THEORY **9+3**

Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition – Toeplitz matrices and some applications.

UNIT III ONE DIMENSIONAL RANDOM VARIABLES **9+3**

Random variables – Probability function- moments –moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions –Functions of a random variable.

UNIT IV DYNAMIC PROGRAMMING **9+3**

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V QUEUEING MODELS **9+3**

Poisson Process – Markovian queues – Single and Multi-server Models – Little'sformula-Machine Interference Model –Steady State analysis –Self Service queue.

T=15; TOTAL: 60 PERIODS

OUTCOMES:

Students should be able to:

1. Solve mathematical problems using analytical methods.
2. Recognize the relationships between different areas of mathematics and the connections between mathematics and Electronic Engineering.
3. Give clear and organized written and verbal explanations of mathematical ideas to a variety of real time technical problems.

REFERENCES:

1. George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and Applications, Prentice Hall of India Pvt. Ltd., 1997.
2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal Processing, Pearson Education, 2000.
3. Richard Johnson, Miller & Freund's Probability and Statistics for Engineers, 7th Edition, Prentice – Hall of India, Private Ltd., New Delhi (2007).

4. Taha, H.A., Operations Research, An introduction, 7th edition, Pearson Education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, Fundamentals of Queuing theory, 2nd Edition, John Wiley and Sons, New York (1985).

CU16103 ADVANCED DIGITAL SIGNAL PROCESSING L T P C
3 1 0 4

OBJECTIVES:

- The purpose of this course is to provide in-depth treatment on methods and techniques in Discrete-time signal transforms, digital filter design, optimal filtering, Power spectrum estimation, multi-rate digital signal processing.
- DSP architectures which are of importance in the areas of signal processing, control and communications.

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 9+3

Weiner Khitchine relation - Power spectral density – filtering random process, Spectral Factorization Theorem, special types of random process – Signal modeling-Least Squares method, Pade approximation, Prony's method, iterative Prefiltering, Finite Data records, Stochastic Models.

UNIT II SPECTRUM ESTIMATION 9+3

Non-Parametric methods - Correlation method - Co-variance estimator - Performance analysis of estimators – Unbiased consistent estimators - Periodogram estimator - Barlett spectrum estimation - Welch estimation - Model based approach - AR, MA, ARMA Signal modeling - Parameter estimation using Yule-Walker method.

UNIT III LINEAR ESTIMATION AND PREDICTION 9+3

Maximum likelihood criterion - Efficiency of estimator - Least mean squared error criterion - Wiener filter - Discrete Wiener Hoff equations - Recursive estimators - Kalman filter - Linear prediction, Prediction error - Whitening filter, Inverse filter - Levinson recursion, Lattice realization, Levinson recursion algorithm for solving Toeplitz system of equations.

UNIT IV ADAPTIVE FILTERS 9+3

FIR Adaptive filters - Newton's steepest descent method - Adaptive filters based on steepest descent method - Widrow Hoff LMS Adaptive algorithm - Adaptive channel equalization - Adaptive echo canceller - Adaptive noise cancellation - RLS Adaptive filters - Exponentially weighted RLS - Sliding window RLS - Simplified IIR LMS Adaptive filter.

UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING 9+3

Mathematical description of change of sampling rate - Interpolation and Decimation -Continuous time model - Direct digital domain approach - Decimation by integer factor -Interpolation by an integer factor - Single and multistage realization - Poly phase realization -Applications to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.

T=15; TOTAL: 60 PERIODS

OUTCOMES:

Students should be able to:

- To design adaptive filters for a given application
- To design multirate DSP systems.

REFERENCES:

1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons Inc., New York, 2006.
2. Sophoncles J. Orfanidis, "Optimum Signal Processing ", McGraw-Hill, 2000.
3. John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Prentice Hall of India, New Delhi, 2005.
4. Simon Haykin, "Adaptive Filter Theory", Prentice Hall, Englehood Cliffs, NJ1986.
5. S. Kay," Modern Spectrum Estimation Theory And Application", Prentice Hall, Englehood Cliffs, Nj1988.
6. P. P. Vaidyanathan, "Multirate Systems And Filter Banks", Prentice Hall, 1992.

AL16101 ADVANCED DIGITAL LOGIC SYSTEM DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

- To analyze synchronous and asynchronous sequential circuits
- To realize and design hazard free circuits
- To familiarize the practical issues of sequential circuit design
- To gain knowledge about different fault diagnosis and testing methods
- To know about timing analysis of memory and PLD

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Networks (CSSN) - Modeling of CSSN – State Assignment and Reduction – Design of CSSN – Design of Iterative Circuits– ASM Chart – ASM Realization, Design of Arithmetic circuits for Fast adder- Array Multiplier.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Design of Hazard free circuits – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits. Practical issues such as clock skew, synchronous and asynchronous inputs and switch bouncing.

UNIT III FAULT DIAGNOSIS & TESTING 9

Fault diagnosis: Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm. Design for testability:Test Generation – Masking Cycle – DFT Schemes. Circuit testing fault model, specific and random faults, testing of sequential circuits, Built in Self Test, Built in Logic Block observer (BILBO), signature analysis.

UNIT IV PERFORMANCE ESTIMATION 9

Estimating digital system reliability, transmission lines, reflections and terminations, system integrity, network issues for digital systems, formal verifications of digital system: model checking, binary decision diagram, theorem proving, circuit equivalence.

UNIT V TIMING ANALYSIS 9

ROM timings, Static RAM timing, Synchronous Static RAM and it's timing, Dynamic RAM timing, Complex Programmable Logic Devices, Logic Analyzer Basic Architecture, Internal structure, Data display, Setup and Control, Clocking and Sampling.

TOTAL:45 PERIODS

OUTCOMES:

- Analyze and design sequential digital circuits
- Identify the requirements and specifications of the system required for a given application

Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:

1. Daniel Tabak , ‘’Advanced Microprocessors” McGraw Hill.Inc., 1995.
2. James L. Antonakos , “ The Pentium Microprocessor ‘’ Pearson Education , 1997.
3. Steve Furber, ‘’ ARM System –On –Chip architecture “Addision Wesley , 2000.
4. Gene .H.Miller .” Micro Computer Engineering ,” Pearson Education , 2003.
5. John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.
6. James L.Antonakos ,” An Introduction to the Intel family of Microprocessors ‘’ Pearson Education 1999.

7. Barry.B.Breg," The Intel Microprocessors Architecture, Programming and Interfacing ", PHI, 2002.
8. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001.
9. Charles J. Sipil, Microcomputer Handbook McCrindle- Collins Publications 1977.

AL16102 ADVANCED MICROPROCESSOR AND MICROCONTROLLER

L	T	P	C
3	0	0	3

OBJECTIVES:

- To familiarize the fundamental concepts of microprocessor architecture.
- To gain knowledge about high performance CISC and RISC architectures.
- To study about 8 bit Microcontrollers viz. 68HC11 and PIC.

UNIT I OVERVIEW **9**

Generic Architecture--Instruction Set – Data formats –Addressing modes – Memory hierarchy – register file –Cache – Virtual memory and paging – Segmentation- pipelining – the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM **9**

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set addressing modes – Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM **9**

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set-Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV MOTOROLA 68HC11 MICROCONTROLLERS **9**

Instruction set addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART.

UNIT V PIC MICROCONTROLLER **9**

CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter – PWM and introduction to C-Compilers.

TOTAL: 45 PERIODS

OUTCOMES:

Students will be able:

- To understand the internal organization of advanced microprocessors and microcontrollers.
- To discriminate the performance of pipe-lining and non-pipe-lining architecture of microprocessors.
- To design an automated system with programming module from the knowledge gained from CISC and RISC architecture.

REFERENCES:

1. Daniel Tabak , “Advanced Microprocessors” McGraw Hill.Inc., 1995.
2. James L. Antonakos , “ The Pentium Microprocessor” Pearson Education, 1997.
3. Steve Furber, “ARM System –On –Chip architecture” Addision Wesley, 2000.
4. Gene .H.Miller “Micro Computer Engineering”, Pearson Education, 2003.
5. John .B.Peatman, “Design with PIC Microcontroller, Prentice hall, 1997.

6. James L.Antonakos, “An Introduction to the Intel family of Microprocessors” Pearson Education 1999.
7. Barry.B.Breg, “The Intel Microprocessors Architecture, Programming and Interfacing”, PHI, 2002.
8. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001.

AL16111 ELECTRONICS SYSTEM DESIGN LABORATORY I

L	T	P	C
0	0	3	2

OBJECTIVES:

- To learn ALP concepts for microprocessor and microcontroller based systems design.
- To study the signal processing concepts.
- To learn HDL program to design digital systems.

LIST OF EXPERIMENTS:

1. System design using PIC, MSP430, ‘51 Microcontroller and 16- bit Microprocessor -8086.
2. Study of different interfaces (using embedded microcontroller)
3. Implementation of Adaptive Filters and multistage multirate system in DSP Processor
4. Simulation of QMF using Simulation Packages
5. Analysis of Asynchronous and clocked synchronous sequential circuits
6. Built in self test and fault diagnosis
7. Sensor design using simulation tools
8. Design and analysis of real time signal processing system – Data acquisition and signal processing

TOTAL: 45 PERIODS

COURSE OUTCOME:

Students will be able to

- Design and implement programs on microprocessor and microcontroller based systems.
- Design and implement signal processing concept in DSP processor.
- Design and test the digital based system using FPGA.
- Design sensors using simulation tools.

AL16201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

L	T	P	C
3	0	0	3

OBJECTIVES:

- To design the single stage amplifiers using pmos and nmos driver circuits with different loads.
- To analyze high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
- To study the different types of current mirrors and to know the concepts of voltage and current reference circuits.

UNIT I SINGLE STAGE AMPLIFIERS 9

Common source stage, Source follower, Common gate stage, Cascode stage, Single ended and differential operation, Basic differential pair, Differential pair with MOS loads.

UNIT II FREQUENCY RESPONSE AND NOISE ANALYSIS 9

Miller effect ,Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascode stage, Differential pair, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III OPERATIONAL AMPLIFIERS 9

Concept of negative feedback, Effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION 9

General considerations, Multipole systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slewing in two stage Op Amps, and Other compensation techniques.

UNIT V BIASING CIRCUITS 9

Basic current mirrors, cascode current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

TOTAL:45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Determine the device dimensions of MOSFETs.
- Discuss the most important building blocks of all CMOS analog ICs.
- Analyze the basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design.
- Design single and multistage voltage, current and differential amplifiers.

REFERENCES:

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design of

Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill, 2001 3. Willey M.C. Sansen, “Analog design essentials”, Springer, 2006.
3. Willey M.C. Sansen, “Analog design essentials”, Springer, 2006.
4. Grebene, “Bipolar and MOS Analog Integrated circuit design”, John Wiley & sons, Inc., 2003.
5. Phillip E.Allen, DouglasR.Holberg, “CMOS Analog Circuit Design”, Second edition, Oxford University Press, 2002.

AL16202 **ASIC AND FPGA DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- To study the design flow of different types of ASIC.
- To familiarize the different types of programming technologies and logic devices.
- To learn the architecture of different types of FPGA.
- To gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC.
- To analyse the synthesis, Simulation and testing of systems.
- To understand the design issues of SOC.
- To know about different high performance algorithms and its applications in ASICs.

UNIT I OVERVIEW OF ASIC AND PLD 9

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs.

UNIT II ASIC PHYSICAL DESIGN 9

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing : global routing - detailed routing - special routing - circuit extraction – DRC.

UNIT III LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT IV FPGA 9

Field Programmable gate arrays- Logic blocks, routing architecture, Design flow technology - mapping for FPGAs, Xilinx XC4000 - ALTERA's FLEX 8000/10000, ACTEL's ACT-1,2,3 and their speed performance Case studies: Altera MAX 5000 and 7000 - Altera MAX 9000 – Spartan II and Virtex II FPGAs - Apex and Cyclone FPGAs.

UNIT V SoC DESIGN 9

Design Methodologies – Processes and Flows - Embedded software development for SOC – Techniques for SOC Testing – Configurable SOC – Hardware / Software codesign Case studies: Digital camera, Bluetooth radio / modem, SDRAM and USB.

TOTAL:45 PERIODS

OUTCOMES:

- Demonstrate VLSI design-flow and appreciate FPGA architecture and to familiarize the different types of programming technologies and logic devices.
- Understand the architecture of different types of FPGA and introduce the principles of design logic cells, I/O cells and interconnect architecture, with equal importance given to FPGA and ASIC styles and also to understand the algorithms used for partitioning, floor planning, and placement and routing during ASIC construction.
- Understand and analyze the synthesis, Simulation and testing of systems.
- Understand the basics of System on Chip and platform based design.

REFERENCES:

1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997
2. S. Trimberger, Field Programmable Gate Array Technology, Edr, Kluwer Academic Publications, 1994.
3. John V.Oldfield, Richard C Dore, Field Programmable Gate Arrays, Wiley Publications 1995.
4. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall, 1994.
5. Parag.K.Lala, Digital System Design using Programmable Logic Devices , BSP, 2003
6. S. Brown, R. Francis, J. Rose, Z. Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
7. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995. 8. Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.
8. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
9. R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House Publishers, 2000.
10. F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs). Prentice Hall PTR, 1999.

AL16203	EMBEDDED SYSTEMS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To afford awareness about Hardware and software design architecture for embedded processors with real time examples.
- To learn various techniques of system design.

UNIT I INTRODUCTION 9

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.

UNIT II EMBEDDED PROCESSORS 9

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus,Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture.

UNIT III DISTRIBUTED EMBEDDED ARCHITECTURE 9

Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS 9

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Offline Versus On-line scheduling.

UNIT V SYSTEM DESIGN TECHNIQUES 9

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

TOTAL:45 PERIODS

OUTCOMES:

Able to select and design suitable embedded systems for real world applications.

REFERENCES:

1. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers, 2008.
2. Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia, 2000.
3. C. M. Krishna and K. G. Shin, “Real-Time Systems” , McGraw-Hill, 1997.

4. Frank Vahid and Tony Givargis, “Embedded System Design: A Unified Hardware/Software Introduction”, John Wiley & Sons, 2006.

CP16103	MULTICORE ARCHITECTURES	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the recent trends in the field of Computer Architecture and identify performance related parameters.
- To appreciate the need for parallel processing.
- To expose the students to the problems related to multiprocessing.
- To understand the different types of multicore architectures.
- To expose the students to warehouse-scale and embedded architectures.

UNIT I FUNDAMENTALS OF QUANTITATIVE DESIGN AND ANALYSIS 9

Classes of Computers – Trends in Technology, Power, Energy and Cost – Dependability – Measuring, Reporting and Summarizing Performance – Quantitative Principles of Computer Design – Classes of Parallelism - ILP, DLP, TLP and RLP - Multithreading - SMT and CMP Architectures – Limitations of Single Core Processors - The Multicore era – Case Studies of Multicore Architectures.

UNIT II DLP IN VECTOR, SIMD AND GPU ARCHITECTURES 9

Vector Architecture - SIMD Instruction Set Extensions for Multimedia – Graphics Processing Units - Detecting and Enhancing Loop Level Parallelism - Case Studies.

UNIT III TLP AND MULTIPROCESSORS 9

Symmetric and Distributed Shared Memory Architectures – Cache Coherence Issues -Performance Issues – Synchronization Issues – Models of Memory Consistency -Interconnection Networks – Buses, Crossbar and Multi-stage Interconnection Networks.

UNIT IV RLP AND DLP IN WA REHOUSE-SCALE ARCHITECTURES 9

Programming Models and Workloads for Warehouse-Scale Computers – Architectures for Warehouse-Scale Computing – Physical Infrastructure and Costs – Cloud Computing – Case Studies.

UNIT V ARCHITECTURES FOR EMBEDDED SYSTEMS 9

Features and Requirements of Embedded Systems – Signal Processing and Embedded Applications – The Digital Signal Processor – Embedded Multiprocessors - Case Studies.

TOTAL:45 PERIODS

OUTCOMES:

Upon completion of the course, the students will be able to

- Identify the limitations of ILP and the need for multicore architectures.
- Discuss the issues related to multiprocessing and suggest solutions.
- Point out the salient features of different multicore architectures and how they exploit parallelism.
- Critically analyze the different types of inter connection networks.
- Discuss the architecture of GPUs, warehouse-scale computers and embedded processors.

REFERENCES:

1. John L. Hennessey and David A. Patterson, “Computer Architecture – A Quantitative Approach”, Morgan Kaufmann / Elsevier, 5th edition, 2012.
2. Kai Hwang, “Advanced Computer Architecture”, Tata McGraw-Hill Education, 2003
3. Richard Y. Kain, “Advanced Computer Architecture a Systems Design Approach”, Prentice Hall, 2011.
4. David E. Culler, Jaswinder Pal Singh, “Parallel Computing Architecture: A Hardware/ Software Approach”, Morgan Kaufmann / Elsevier, 1997.

AL16211	ELECTRONICS SYSTEM DESIGN LABORATORY II	L	T	P	C
		0	0	3	2

OBJECTIVES:

- To introduce the programming concepts using Verilog or VHDL
- To introduce the concepts of system design using FPGA

LIST OF EXPERIMENTS:

1. Study of 32 bit ARM7 microcontroller RTOS and its application.
2. Testing RTOS environment and system programming.
3. Designing of wireless network using embedded systems.
4. Implementation of ARM with FPGA.
5. Design and Implementation of ALU in FPGA using VHDL and Verilog.
6. Modeling of Sequential Digital system using Verilog and VHDL.
7. Flash controller programming – data flash with erase, verify and fusing.
8. System design using ASIC.
9. Design, simulation and analysis of signal integrity

TOTAL: 45 PERIODS

OUTCOME:

Ability to develop FPGA based system design.

ELECTIVE I

CU16005	ADVANCED DIGITAL IMAGE PROCESSING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the image fundamentals and mathematical transforms necessary for image processing and to study the image enhancement techniques.
- To understand the image segmentation and representation techniques.
- To understand how image are analyzed to extract features of interest.
- To introduce the concepts of image registration and image fusion.
- To analyze the constraints in image processing when dealing with 3D data sets.

UNIT I FUNDAMENTALS OF DIGITAL IMAGE PROCESSING 9

Elements of visual perception, brightness, contrast, hue, saturation, mach band effect, 2D image transforms-DFT, DCT, KLT, and SVD. Image enhancement in spatial and frequency domain, Review of morphological image processing

UNIT II SEGMENTATION 9

Edge detection, Thresholding, Region growing, Fuzzy clustering, Watershed algorithm, Active contour methods, Texture feature based segmentation, Model based segmentation, Atlas based segmentation, Wavelet based Segmentation methods

UNIT III FEATURE EXTRACTION 9

First and second order edge detection operators, Phase congruency, Localized feature extraction-detecting image curvature, shape features Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors- Autocorrelation, Co-occurrence features, Runlength features, Fractal model based features, Gabor filter, wavelet features

UNIT IV REGISTRATION AND IMAGE FUSION 9

Registration- Preprocessing, Feature selection-points, lines, regions and templates Feature correspondence-Point pattern matching, Line matching, region matching Template matching .Transformation functions-Similarity transformation and Affine Transformation. Resampling-Nearest Neighbour and Cubic Splines Image Fusion-Overview of image fusion, pixel fusion, Multiresolution based fusion discrete wavelet transform, Curvelet transform. Region based fusion.

UNIT V 3D IMAGE VISUALIZATION 9

Sources of 3D Data sets, Slicing the Data set, Arbitrary section planes, The use of color, Volumetric display, Stereo Viewing, Ray tracing, Reflection, Surfaces, Multiply connected surfaces, Image processing in 3D, Measurements on 3D images.

TOTAL: 45 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to

- To understand image formation and the role human visual system plays in perception of gray and color image data.
- To apply image processing techniques in both the spatial and frequency (Fourier) domains.

- To design image analysis techniques in the form of image segmentation and to evaluate the methodologies for segmentation.
- To conduct independent study and analysis of feature extraction techniques.
- To understand the concepts of image registration and image fusion.
- To analyze the constraints in image processing when dealing with 3D data sets and to apply image processing algorithms in practical applications.

TEXT BOOKS:

1. John C.Russ, "The Image Processing Handbook", CRC Press, 2007.
2. Mark Nixon, Alberto Aguado, "Feature Extraction and Image Processing", Academic Press, 2008.
3. Ardeshir Goshtasby, "2D and 3D Image registration for Medical, Remote Sensing and Industrial Applications", John Wiley and Sons, 2005.

REFERENCES:

1. Rafael C. Gonzalez, Richard E. Woods, "Digital Image Processing", Pearson, Education, Inc., Second Edition, 2004.
2. Anil K. Jain, "Fundamentals of Digital Image Processing", Pearson Education, Inc., 2002.
3. Rick S.Blum, Zheng Liu, "Multisensor image fusion and its Applications", Taylor& Francis, 2006.

CU16007 WAVELET TRANSFORMS AND APPLICATIONS L T P C
3 0 0 3

OBJECTIVES:

- To study the basics of signal representation and Fourier theory
- To understand Multi Resolution Analysis and Wavelet concepts
- To study the wavelet transform in both continuous and discrete domain
- To understand the design of wavelets using Lifting scheme
- To understand the applications of Wavelet transform.

UNIT I FUNDAMENTALS 9

Vector Spaces – Properties– Dot Product – Basis – Dimension, Orthogonality and Orthonormality – Relationship Between Vectors and Signals – Signal Spaces – Concept of Convergence – Hilbert Spaces for Energy Signals- Fourier Theory: Fourier series expansion, Fourier transform, Short time Fourier transform, Time-frequency analysis.

UNIT II MULTI RESOLUTION ANALYSIS 9

Definition of Multi Resolution Analysis (MRA) – Haar Basis – Construction of General Orthonormal MRA – Wavelet Basis for MRA – Continuous Time MRA Interpretation for the DTWT – Discrete Time MRA – Basis Functions for the DTWT – PRQMF Filter Banks.

UNIT III CONTINUOUS WAVELET TRANSFORMS 9

Wavelet Transform – Definition and Properties – Concept of Scale and its Relation with Frequency – Continuous Wavelet Transform (CWT) – Scaling Function and Wavelet Functions (Daubechies Coiflet, Mexican Hat, Sinc, Gaussian, Bi Orthogonal)– Tiling of Time – Scale Plane for CWT.

UNIT IV DISCRETE WAVELET TRANSFORM 9

Filter Bank and Sub Band Coding Principles – Wavelet Filters – Inverse DWT Computation by Filter Banks – Basic Properties of Filter Coefficients – Choice of Wavelet Function Coefficients – Derivations of Daubechies Wavelets – Mallat's Algorithm for DWT –Multi Band Wavelet Transforms Lifting Scheme- Wavelet Transform Using Polyphase Matrix Factorization – Geometrical Foundations of Lifting Scheme – Lifting Scheme in Z –Domain.

UNIT V APPLICATIONS 9

Wavelet methods for signal processing- Image Compression Techniques: EZW–SPHIT Coding – Image Denoising Techniques: Noise Estimation – Shrinkage Rules – Shrinkage Functions – Edge Detection and Object Isolation, Image Fusion, and Object Detection.

TOTAL: 45 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to

- Use Fourier tools to analyse signals
- Gain knowledge about MRA and representation using wavelet bases
- Acquire knowledge about various wavelet transforms and design wavelet transform
- Apply wavelet transform for various signal & image processing applications.

TEXT BOOKS:

1. Rao R M and A S Bopardikar, ―Wavelet Transforms Introduction to theory and Applications, Pearson Education, Asia, 2000.
2. L.Prasad & S.S.Iyengar, Wavelet Analysis with Applications to Image Processing, CRC Press, 1997.

REFERENCES:

1. J. C. Goswami and A. K. Chan, "Fundamentals of wavelets: Theory, Algorithms and Applications" Wiley Interscience Publication, John Wiley & Sons Inc., 1999.
2. M. Vetterli, J. Kovacevic, "Wavelets and subband coding" Prentice Hall Inc, 1995.
3. Stephen G. Mallat, "A wavelet tour of signal processing" 2nd Edition Academic Press, 2000.
4. Soman K P and Ramachandran K I, ―Insight into Wavelets From Theory to practice, Prentice Hall, 2004.

CP16036	SOFT COMPUTING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn the key aspects of Soft computing and Neural networks.
- To know about the components and building block hypothesis of Genetic algorithm.
- To understand the features of neural network and its applications
- To study the fuzzy logic components
- To gain insight onto Neuro Fuzzy modeling and control
- To gain knowledge in machine learning through Support vector machines.

UNIT I INTRODUCTION TO SOFT COMPUTING 9

Evolution of Computing - Soft Computing Constituents – From Conventional AI to Computational Intelligence - Machine Learning Basics.

UNIT II GENETIC ALGORITHMS 9

Introduction, Building block hypothesis, working principle, Basic operators and Terminologies like individual, gene, encoding, fitness function and reproduction, Genetic modeling: Significance of Genetic operators, Inheritance operator, cross over, inversion & deletion, mutation operator, Bitwise operator, GA optimization problems, JSPP (Job Shop Scheduling Problem), TSP (Travelling Salesman Problem),Differences & similarities between GA & other traditional methods, Applications of GA.

UNIT III NEURAL NETWORKS 9

Machine Learning using Neural Network, Adaptive Networks – Feed Forward Networks– Supervised Learning Neural Networks – Radial Basis Function Networks - Reinforcement Learning – Unsupervised Learning Neural Networks – Adaptive Resonance Architectures – Advances in Neural Networks.

UNIT IV FUZZY LOGIC 9

Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making.

UNIT V NEURO-FUZZY MODELING 9

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification – Neuro-Fuzzy Control – Case Studies.

TOTAL: 45 PERIODS

OUTCOMES:

- Implement machine learning through Neural networks.
- Develop a Fuzzy expert system.
- Model Neuro Fuzzy system for clustering and classification.
- Write Genetic Algorithm to solve the optimization problem
- Use Support Vector Machine for enabling the machine learning.

REFERENCES:

1. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, “Neuro-Fuzzy and Soft Computing”, Prentice-Hall of India, 2003.
2. Kwang H.Lee, “First course on Fuzzy Theory and Applications”, Springer–Verlag Berlin Heidelberg, 2005.
3. George j. klir and bo yuan, “fuzzy sets and fuzzy logic-theory and applications”, prentice hall, 1995.
4. James a. freeman and david m. skapura, “neural networks algorithms, applications, and programming techniques”, pearson edn., 2003.
5. David e. goldberg, “genetic algorithms in search, optimization and machine learning”, addison wesley, 2007.
6. Mitsuo gen and runwei cheng,”genetic algorithms and engineering optimization”, wiley publishers 2000.
7. Mitchell melanie, “an introduction to genetic algorithm”, prentice hall, 1998.
8. S.N.Sivanandam, s.n.deepa, “introduction to genetic algorithms”, springer, 2007.
9. Eiben and smith “introduction to evolutionary computing” springer.
10. E. Sanchez, t. shibata, and l. a. zadeh, eds., "genetic algorithms and fuzzy logic systems: soft computing perspectives, advances in fuzzy systems - applications and theory", vol. 7 river edge, world scientific, 1997.

AL16001 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

L	T	P	C
3	0	0	3

OBJECTIVES:

- To understand the difference between the pipeline and parallel concepts.
- To study the various types of architectures and the importance of scalable architectures.
- To study the various memories and optimization of memory.

UNIT I COMPUTER DESIGN AND PERFORMANCE MEASURES 9

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors –Multivector and SIMD architectures – Multithreaded architectures – Data-flow architectures -Performance Measures.

UNIT II PARALLEL PROCESSING, PIPELINING AND ILP 9

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors

UNIT III MEMORY HIERARCHY DESIGN 9

Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies.

UNIT IV MULTIPROCESSORS 9

Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency -Interconnection networks – Buses, crossbar and multi-stage switches.

UNIT V MULTI-CORE ARCHITECTURES 9

Software and hardware multithreading – SMT and CMP architectures – Design issues – Case studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture – hp architecture.

TOTAL: 45 PERIODS

OUTCOMES: Students will be able to

- Able to explain the advanced concepts of parallel architecture
- Apply the memory hierarchy for multiprocessor system
- Able to analyze the design structures of pipelined and multiprocessor systems

REFERENCES:

1. Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001.
2. John L. Hennessey and David A. Patterson, “Computer Architecture – A quantitative approach”, Morgan Kaufmann / Elsevier, 4th. edition, 2007.

3. William Stallings, “Computer Organization and Architecture – Designing for Performance”, Pearson Education, Seventh Edition, 2006.
4. John P. Hayes, “Computer Architecture and Organization”, McGraw Hill
5. David E. Culler, Jaswinder Pal Singh, “Parallel Computing Architecture: A hardware/ software approach”, Morgan Kaufmann / Elsevier, 1997.
6. Dimitrios Soudris, Axel Jantsch, "Scalable Multi-core Architectures: Design Methodologies and Tools", Springer, 2012
7. John P. Shen, “Modern processor design. Fundamentals of super scalar processors”, Tata McGraw Hill 2003.

AL16002 THREE DIMENSIONAL NETWORK ON CHIP

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To introduce the concept of 3D NOC.
- To study the architectures and protocols of 3D NOC.
- To identify the types of fault and study the testing methods for fault rectification.
- To learn DimDE router for 3D NOC.

UNIT I INTRODUCTION TO THREE DIMENSIONAL NOC **9**

Three-Dimensional Networks-on-Chips Architectures. – Resource Allocation for QoSOn-Chip Communication – Networks-on-Chip Protocols-On-Chip Processor Traffic Modeling for Networks-on-Chip.

UNIT II TEST AND FAULT TOLERANCE OF NOC **9**

Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on-Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for Networks-on-Chips.

UNIT III ENERGY AND POWER ISSUES OF NOC **9**

Energy and Power Issues in Networks-on-Chips-The CHAIN works Tool Suite: AComplete Industrial Design Flow for Networks-on-Chips.

UNIT IV MICRO-ARCHITECTURE OF NOC ROUTER **9**

Baseline NoC Architecture – MICRO-Architecture Exploration ViChaR: A Dynamic Virtual Channel Regulator for NoC Routers- RoCo: The Row-Column Decoupled Router – A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks. Exploring Fault Tolerant Networks-on-Chip Architectures.

UNIT V DIMDE ROUTER FOR 3D NOC **9**

A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures-Digest of Additional NoC MACRO-Architectural Research.

TOTAL: 45 PERIODS

OUTCOMES: Students will be able to

- Understand the Architecture of 3D NOC.
- Apply the fault tolerant concept for Networks

REFERENCES:

1. Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-on - Chip "Architectures A Holistic Design Exploration", Springer.
2. Fayezgebali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi "Networks-on-Chips theory and practice CRC press.

ELECTIVE II

AL16003	CAD FOR VLSI CIRCUITS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To study various physical design methods in VLSI.
- To understand the concepts behind the VLSI design rules and routing techniques.
- To use the simulation techniques at various levels in VLSI design flow
- To understand the concepts of various algorithms used for floor planning and routing techniques

UNIT I VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms -Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II DESIGN RULES 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation – Placement algorithms – partitioning.

UNIT III FLOOR PLANNING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V MODELLING AND SYNTHESIS 9

High level Synthesis - Hardware models - Internal representation - Allocation -assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TOTAL: 45 PERIODS

OUTCOMES: At the end of the course, the student should be able to:

- Use VLSI design automation tools
- Perform high level synthesis
- Discuss floor planning concepts
- Design algorithms for placement and partitioning

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
3. Sadiq M. Sait, Habib Youssef, “VLSI Physical Design automation: Theory and Practice”, World scientific 1999.
4. Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing 1987.

AL16004 DIGITAL CONTROL ENGINEERING

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To study the principles of PI, PD, PID controllers.
- To analyse time and frequency response discrete time control system
- To familiarize and practice digital control algorithms
- To implement PID control algorithms using microprocessors, microcontrollers.

UNIT I PRINCIPLES OF CONTROLLERS 9

Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9

Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM 9

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9

Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

TOTAL: 45 PERIODS

OUTCOMES:

- Acquire working knowledge of discrete system science-related mathematics.
- Design a discrete system, component or process to meet desired needs.
- Identify, formulate and solve discrete control engineering problems.
- Use the techniques, tools and skills related to discrete signals, computer science and modern discrete control engineering in modern engineering practice
- Communicate system related concepts effectively

REFERENCES:

1. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.
2. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995.
3. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.

AL16005	HARDWARE - SOFTWARE CO DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To acquire the knowledge about system specification and modeling.
- To learn the formulation of partitioning
- To analyze about co-synthesis.
- To study the different technical aspects about prototyping and emulation.
- To formulate the design specification and validate its functionality by simulation.

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems , Hardware/Software Co-Design , Co-Design for System Specification and Modelling , Co-Design for Heterogeneous Implementation – Processor Synthesis , Single-Processor Architectures with one ASIC , Single-Processor Architectures with many ASICs, Multi-Processor Architectures , Comparison of Co- Design Approaches , Models of Computation ,Requirements for Embedded System Specification.

UNIT II HARDWARE/SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping ,Target Architecture-Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems.

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification , Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Cosimulation.

TOTAL: 45 PERIODS

OUTCOMES: On completion of the course, a student should be able:

- To outline and apply design methodologies
- To appreciate the fundamental building blocks of the using hardware and software co-design and related implementation and testing environments and techniques and their inter-relationships
- To modern hardware/software tools for building prototypes

- To demonstrate practical competence in these areas.

REFERENCES:

1. Ralf Niemann , “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup, Wayne Wolf,”Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Pub, 1997.
3. Giovanni De Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design” Kaufmann Publishers, 2001.

AL16006 **QUANTUM ELECTRONICS** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To know the concepts of EM fields and wave equations.
- To study the types of lasers and its characteristics.
- To know the various methods of scattering.
- To learn the concept of Non-linear optics.

UNIT I BASIC THEOREMS AND POSTULATES OF QUANTUM MECHANICS 9

Introduction to Quantum Electronics- Résumé of electromagnetic theory-Waveguides-Planarmirror waveguides-Modes in dielectric slab waveguides-Effective Index Method-Guided wave coupling and interference-Coupled Mode Theory-Directional coupler-Mode coupling in periodic waveguides-Mode interference-The Schrodinger wave equation, some solutions of time independent Schrodinger equation, Matrix formulation of quantum mechanics, Lattice vibration and their quantization, Electromagnetic fields and their quantization.

UNIT II LASER 9

Gaussian beam in a homogenous medium, Gaussian beam in a lens waveguide, Elliptic Gaussian beams, Optical resonators, Spontaneous and induced transitions, gain coefficient, homogenous and inhomogeneous broadening, Laser oscillations, Semiconductor laser, quantum well laser, modulation of optical radiation, Q switching and Mode locking of laser, Quantum wires and dots, Laser arrays, Concept of super modes, Phase amplitude in laser, Free electron lasers.

UNIT III NONLINEAR OPTICS 9

Introduction to nonlinear (NL) optics, 2nd order NL effects-The nonlinear optical susceptibility tensor, Second harmonic generation, parametric oscillations, parametric amplifiers, Applications– Nonlinear polarization –physical origin-Complex notation, conservation laws-Second Harmonic Generation, Birefringence and Quasi- Phase Matching-3rd order NL effects- Self-Phase Modulation, Optical soliton-Stimulated Raman Scattering-Electro-optic (EO) modulation of light-Linear EO effect, Phase retardation-Amplitude, and Phase modulation- Traveling wave modulator.

UNIT IV STIMULATED RAMAN AND BRILLOUIN SCATTERING 9

Stimulated Raman scattering, Antisokes scattering, stimulated Brillouin scattering, self focusing of optical beams.

UNIT V NOISE 9

Noise in laser amplifier and oscillator, Laser spectra, Measurements.

TOTAL: 45 PERIODS

OUTCOMES: Student will be able to

- Understand the concept of EM fields and Wave equations.
- Analyze the various noise effects in amplifier and oscillators.

REFERENCES:

1. Amnon Yariv, “Quantum Electronics”, John Wiley 1989.
2. Max Schubert, Bernd Wilhelmi, “Nonlinear optics and quantum electronics”, Wiley-Interscience 1986.
3. D.Marcuse, “Principle of Quantum Electronics”, Cambridge 1980.
4. David Klyshko, “Physical Foundations of Quantum Electronics”, World Scientific 2011.
5. J.T. Verdeyen, “Laser Electronics”, Prentice-Hall 1995.
6. Harisson Paul, “Quantum Wells, Wires and Dots”, Wiley 2011.
7. G.P.Agarwal and N.K.Dutta, “Long Wavelength Semiconductor lasers”, Van Nostrand Reinhold 1986.
8. A.Yariv, “Optical Electronics”, CBS College Publishing 1984.

AL16007 SENSORS AND SIGNAL CONDITIONING

L	T	P	C
3	0	0	3

OBJECTIVES:

- To know the static and dynamic characteristics of measurement systems.
- To study about the various types of sensors viz. Resistive, Reactive, Self- generating.
- To know the different types digital and semiconductor sensors.

UNIT I INTRODUCTION TO MEASUREMENT SYSTEMS 9

Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction performance characteristics: static characteristics of measurement systems, accuracy, precision, sensitivity, other characteristics: linearity, resolution, systematic errors, random errors, dynamic characteristics of measurement systems: zero-order, first-order, and second-order measurement systems and response

UNIT II RESISTIVE SENSORS 9

Resistive sensors: potentiometers, strain gages and types, resistive temperature detectors (rtds), thermistors, magneto resistors, light-dependent resistors (ldrs); Signal conditioning for resistive sensors: measurement of resistance, voltage dividers , Wheatstone bridge. Balance and deflection measurements , sensor bridge calibration and compensation instrumentation amplifiers , interference types and reduction

UNIT III REACTIVE SENSORS 9

Reactance variation and electromagnetic sensors : capacitive sensors – variable & differential, inductive sensors – reluctance variation, eddy current, linear variable differential transformers (lvdts), variable transformers: synchros, resolvers, inductosyn, magneto elastic sensors, electromagnetic sensors – sensors based on faraday's law, hall effect sensors, Signal conditioning for reactance variation sensors : problems and alternatives, ac bridges, carrier amplifiers – application to the lvdt, variable oscillators, resolver-to-digital and digital-to-resolver converters

UNIT IV SELF-GENERATING SENSORS 9

Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors: chopper and low-drift amplifiers, offset and drifts amplifiers, electrometer amplifiers, charge amplifiers, noise in amplifiers

UNIT V DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS 9

Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wire strain gages , vibrating cylinder sensors, saw sensors, digital flow meters, Sensors based on semiconductor junctions : thermometers based on semiconductor junctions, magneto diodes and magneto transistors, photodiodes and phototransistors, sensors based on mosfet transistors, charge-coupled sensors – types of CCD imaging sensors , ultrasonic-based sensors , fiber-optic sensors

TOTAL: 45 PERIODS

OUTCOMES: Student will be able to

- Classify various measurement systems followed in sensor systems and evaluate its performance.
- Design resistive sensors and identify methodologies to reduce its interference signals
- Design reactive sensors and perform signal conditioning for reactance variation sensors
- Design self generating sensors and perform signal conditioning for the same
- Design digital sensors and semiconductor junction based sensors

REFERENCES:

1. Ramon Pallás Areny, John G. Webster, "Sensors and Signal Conditioning", 2nd edition, John Wiley and Sons, 2000.
2. D.Patranabis, "Sensors and Transducers", TMH 2003.
3. Jon Wilson, "Sensor Technology Handbook", Newne 2004.
4. Herman K.P. Neubrat, "Instrument Transducers – An Introduction to Their Performance and Design", Oxford University Press.
5. E.O. Doeblin, "Measurement System: Applications and Design", McGraw Hill Publications.
6. D. Johnson, "Process Control Instrumentation Technology", John Wiley and Sons.
7. Kevin James, PC Interfacing and Data acquisition, Elsevier, 2011.
8. Graham Brooker, Introduction to Sensors for ranging and imaging, Yesdee, 2009.
9. Ian Sinclair, Sensors and Transducers, Elsevier, 3rd Edition, 2011.

ELECTIVE III

AL16008	VLSI DESIGN TECHNIQUES	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the concepts of MOS transistors operations and their AC , DC characteristics
- To know the fabrication process of cmos technology and its layout design rules
- To understand the latch up problem in cmos circuits.
- To study the concepts of cmos inverters and their sizing methods
- To know the concepts of power estimation and delay calculations in cmos circuits.

UNIT I MOS TRANSISTOR THEORY 9

NMOS and PMOS transistors, CMOS logic, MOS transistor theory – Introduction, Enhancement mode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model.

UNIT II CMOS TECHNOLOGY AND DESIGN RULE 9

CMOS fabrication and Layout, CMOS technologies, P -Well process, N -Well process, twin – tub process, MOS layers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS process enhancements, Technology – related CAD issues, Fabrication and packaging.

UNIT III INVERTERS AND LOGIC GATES 9

NMOS and CMOS Inverters, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT IV CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT V VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits –Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.

TOTAL: 45 PERIODS

OUTCOMES: At the end of the course, the student should be able to:

- Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.
- Discuss design methodology of arithmetic building block

- Analyze the various VLSI component circuit.

REFERENCES:

1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2. John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc., 2002.
3. Eugene D.Fabricius, Introduction to VLSI Design McGraw Hill International Editions, 1990.
4. Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 1995.
5. Wayne Wolf "Modern VLSI Design System on chip. Pearson Education.2002.

AL16009 **LOW POWER VLSI DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- To know the sources of power consumption in cmos circuits.
- To understand the various power reduction techniques and the power estimation methods.
- To study the design concepts of low power circuits.

UNIT I POWER DISSIPATION 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation inCMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.8

UNIT III DESIGN OF LOW POWER CIRCUITS 9

Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION 9

Power Estimation technique – logic power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN 9

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

OUTCOMES:

- The student will apply the basics and advanced techniques in low power design which is a hot topic in today‟s market where the power plays major role.
- The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

REFERENCES:

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
2. Dimitrios Soudris, Christians Pignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002
3. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995.
5. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001.
8. Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing.

AL16010	FIBER OPTIC SENSORS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To familiarize about fiber optic sensor technology.
- To study about Optical resonators.
- To acquire knowledge about magnetic sensors.
- To know about Chemical and Biosensors.
- To gain knowledge about smart structures.

UNIT I SENSOR TECHNOLOGY 9

The Emergence of Fiber Optic Sensor Technology-Optical Fibers-Light Sources-Optical Detectors-Optical Modulators- Intensity-Based and Interferometric Sensors-Fabry perot, Mach Zender, Michelson and Sagnac.

UNIT II GRATING SENSORS 9

Multimode Grating and Polarisation Sensors-Sensors Based on Relative Movement of Opposed Gratings-Grating Period Modulation-Sensors Based on the Photoelastic Effect-Retardation Plates-Fiber Grating Sensors.

UNIT III DISTRIBUTED AND MAGNETIC SENSORS 9

Fiber Optic Distributed and Magnetic Sensor-Distributed Sensing- Basic Principles of Sensor Multiplexing- Interferometric Sensor Multiplexing- Faraday effect sensors-Magneto strictive - Lorentz force sensors-Evanescent Field Absorption Sensors.

UNIT IV CHEMICAL AND BIOSENSOR 9

Fiber Optic Chemical and Biosensor: Reagent Mediated sensor-Humidity sensor – pH sensor - Hydrogen sensor - CO2 sensor – Ammonia sensor - Chloride sensor – Glucose sensor – Oxygen sensor - Surface Plasmonic Resonance based sensor.

UNIT V APPLICATIONS 9

Industrial Applications of Fiber Optic Sensors : Temperature – Pressure - fluid level – flow – position - vibration - rotation measurements - Current -voltage measurement – Chemical analysis. Introduction to smart structures - Applications –skins.

TOTAL: 45 PERIODS

OUTCOMES: Student will be able to

- Understand the various types of sensors in fiber optics.

REFERENCES:

1. Eric Udd, William B. Spillman, Jr., “Fiber Optic Sensors: An Introduction for Engineers and Scientists”, John Wiley & Sons 2011.
2. Bhagavānadāsa Gupta, Banshi Das Gupta, “Fiber Optic Sensors: Principles and Applications”, New India Publishing 2006.
3. David A. Krohn, “Fiber optic sensors: fundamentals and applications”, ISA Publishing 2000.
4. Francis T.S. Yu, Shizhuo Yin, Paul B. Ruffin, “Fiber Optic Sensors”, CRC Press Publisher 2010.

5. B.Culshaw and J.Daykin, “Optic fiber Sensors Systems and Applications”, Artech House 1989.
6. KTV Grattan & BT Meggit, “Optical fiber sensor technology & Applications”, Kluwer Academic 2000.

AL16011 DSP INTEGRATED CIRCUITS L T P C

3 0 0 3

OBJECTIVES:

- To study the procedural flow of system design in DSP and Integrated circuit.
- To analyse the frequency response and transfer function of DSP systems.
- To compare and study the performance of various transforms for signal processing.
- To design FIR and IIR filters for the given specifications.
- To study the architectures for DSP system.
- To study the design layout for VLSI circuits.

UNIT I DSP INTEGARTED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT II DIGITAL SIGNAL PROCESSING 9

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

UNIT V ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. Cordic algorithm.

TOTAL: 45 PERIODS

OUTCOMES:

- Get to know about the Digital Signal Processing concepts and it‟s algorithms
- Get an idea about finite wordlength effects in digital filters
- Concept behind multirate systems is understood.
- Get familiar with the DSP processor architectures and how to perform synthesis of processing elements
- Acquire an general idea about VLSI circuit layout design aspects

REFERENCES:

1. Lars Wanhammer, “DSP Integrated Circuits”, 1999 Academic press, New York
2. A.V.Oppenheim et.al, “Discrete-time Signal Processing”, Pearson Education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, “Digital signal processing – A practical approach”, Second Edition, Pearson Education, Asia.
4. Keshab K.Parhi, “VLSI Digital Signal Processing Systems design and Implementation”, John Wiley & Sons, 1999.

CU16016 **RF SYSTEM DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- To learn the importance and issues in the design of RF
- To design RF filter and RF amplifier
- To study about the characteristics of oscillators, mixers, PLL, wireless synthesizers and detector circuits.

UNIT I RF ISSUES **9**

Importance of RF design- Electromagnetic spectrum, RF behavior of passive components, chip components and circuit board considerations, scattering parameters, smith chart and applications.

UNIT II RF FILTER DESIGN **9**

Overview, Basic resonator and filter configuration, special filter realizations, smith chart based filter design, coupled filter.

UNIT III ACTIVE RF COMPONENTS AND APPLICATIONS **9**

RF diodes, BJT, RF FET'S, High electron mobility transistors, matching and biasing networks impedance matching using discrete components, microstripline matching networks, amplifier classes of operation and biasing networks.

UNIT IV RF AMPLIFIER DESIGNS **9**

Characteristics, amplifier power relations, stability considerations, constant gain circles, constant VSWR circles, low noise circles broadband, high power and multistage amplifiers.

UNIT V OSCILLATORS, MIXERS & APPLICATIONS **9**

Basic oscillator model, High Frequency oscillator configuration, basic characteristic of mixers, wireless synthesizers, phase locked loops, detector and demodulator circuits.

TOTAL: 45 PERIODS

OUTCOMES:

- The student after completing this course must be able to translate the top level wireless communications system specifications into block level specifications of the RFE.
- The student should also able to carry out transistor level design of the entire RFE

REFERENCES:

1. Reinhold Ludwig and Powel Bretchko, RF Circuit Design – Theory and Applications, Pearson Education Asia, First Edition, 2001.
2. Joseph. J. Carr, Secrets of RF Circuit Design , McGraw Hill Publishers, Third Edition, 2000.
3. Mathew M. Radmanesh, Radio Frequency & Microwave Electronics, Pearson Education Asia, Second Edition, 2002.
4. Ulrich L. Rohde and David P. NewKirk, RF / Microwave Circuit Design, John Wiley & Sons USA 2000.
5. Roland E. Best, Phase - Locked Loops: Design, simulation and applications, McGraw Hill Publishers 5TH edition 2003.

AL16012 ANALOG AND MIXED MODE VLSI DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

- To study the concepts of MOS large signal model and small signal model
- To understand the concepts of D/A conversion methods and their architectures.
- To design filters for ADC.
- To study about the switched capacitor circuits.

UNIT I INTRODUCTION AND BASIC MOS DEVICES 9

Challenges in analog design-Mixed signal layout issues- MOS FET structures and characteristics-large signal model – small signal model- single stage Amplifier-Source follower- Common gate stage – Cascode Stage.

UNIT II SIBMICRON CIRCUIT DESIGN 9

Submicron CMOS process flow, Capacitors and resistors, Current mirrors, Digital Circuit Design, Delay Elements – Adders- OP Amp parameters and Design.

UNIT III DATA CONVERTERS 9

Characteristics of Sample and Hold- Digital to Analog Converters- architecture-Differential Non linearity-Integral Non linearity- Voltage Scaling-Cyclic DAC-Pipeline DAC-Analog to Digital Converters- architecture – Flash ADC-Pipeline ADC-Differential Non linearity-Integral Non linearity.

UNIT IV SNR IN DATA CONVERTERS 9

Overview of SNR of Data Converters- Clock Jitters- Improving Using Averaging – Decimating Filters for ADC- Band pass and High Pass Sinc Filters- Interpolating Filters for DAC.

UNIT V SWITCHED CAPACITOR CIRCUITS 9

Resistors, First order low pass Circuit, Switched capacitor Amplifier, Switched Capacitor Integrator.

TOTAL: 45 PERIODS

OUTCOMES: Student will be able to

- Student will be able to analyze MOS analog circuits using small signal model and large signal model
- Students will be able to design and implement submicron digital circuits
- Students will be able to design,implement and analyze the characteristics of data converters, digital filters and switched capacitor circuits

REFERENCES:

1. Vineetha P.Gejji Analog and Mixed Mode Design - Prentice Hall, 1st Edition, 2011.
2. Jeya Gowri Analog and Mixed Mode Design- Sapna publishing House 2011.

ELECTIVE IV

AL16013	ANALOG VLSI DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To study the concepts of CMOS and BICMOS analog circuits.
- To understand the concepts of A/D convertors and analog integrated sensors.
- To understand the testing concepts in analog VLSI circuits and its statistical modeling.

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW VOLTAGESIGNAL PROCESSING **9**

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells-Linear Voltage- Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op- Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT –MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING **9**

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS **9**

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma- Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS **9**

Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron -Beam Testablity-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT **9**

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL: 45 PERIODS

OUTCOMES: Student will be able to

- Understand the various testing methods in analog VLSI circuit.
- Analyze the various Layout design rules.

REFERENCES:

1. Mohammed Ismail, Terri Fief, “Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May, “Analog VLSI Design - NMOS and CMOS ", Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsividis, “Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994.

AL16014 PHYSICAL DESIGN OF VLSI CIRCUITS

L	T	P	C
3	0	0	3

OBJECTIVES:

- To introduce the physical design concepts such as routing, placement, partitioning and packaging and to study the performance of circuits layout designs, compaction techniques.

UNIT I INTRODUCTION TO VLSI TECHNOLOGY 9

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies Packaging-Computational Complexity-Algorithmic Paradigms.

UNIT II PLACEMENT USING TOP-DOWN APPROACH 9

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut partition with capacity and i/o constrants. Floor planning: Rectangular dual floor planning hierarchial approach- simulated annealing- Floor plan sizing Placement: Cost function- force directed method- placement by simulated annealing partitioning placement- module placement on a resistive network – regular placement linear placement.

UNIT III ROUTING USING TOP DOWN APPROACH 9

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches-hierarchial approaches- multi commodity flow based techniques- Randomised Routing- One Step approach- Integer Linear Programming Detailed Routing: Channel Routing- Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs.

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT 9

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem-Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization.

UNIT V SINGLE LAYER ROUTING,CELL GENERATION AND COMPACTION 9

Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing-Wire length and bend minimization technique – Over The Cell (OTC) Routing Multiple chip modules(MCM)- programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

TOTAL: 45 PERIODS

OUTCOMES: Student will be able to

- Differentiate various layout rules used in VLSI technology
- Perform partitioning and floor planning using top down approach in VLSI
- Apply optimised routing process FPGA design
- Troubleshoot various performance issues in VLSI circuits

- Apply routing for single layer and multiple chip modules in VLSI design

REFERENCES:

1. Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", Mc Graw Hill International Edition 1995.
2. Preas M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.

AL16015 VLSI SIGNAL PROCESSING

L	T	P	C
3	0	0	3

OBJECTIVES:

- To understand the various VLSI architectures for digital signal processing.
- To know the techniques of critical path and algorithmic strength reduction in the filter structures.
- To study the performance parameters, viz. area, speed and power.

UNIT I INTRODUCTION **6**

Overview of DSP – FPGA Technology – DSP Technology requirements – Design Implementation.

UNIT II METHODS OF CRITICAL PATH REDUCTION **12**

Binary Adders – Binary Multipliers – Multiply-Accumulator (MAC) and sum of product (SOP) – Pipelining and parallel processing – retiming – unfolding – systolic architecture design.

UNIT III ALGORITHMIC STRENGTH REDUCTION METHODS AND RECURSIVE FILTER DESIGN **9**

Fast convolution-pipelined and parallel processing of recursive and adaptive filters – fast IIR filters design.

UNIT IV DESIGN OF PIPELINED DIGITAL FILTERS **9**

Designing FIR filters – Digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic – scaling and round-off noise.

UNIT V SYNCHRONOUS ASYNCHRONOUS PIPELINING AND PROGRAMMABLE DSP **9**

Numeric strength reduction – synchronous – wave and asynchronous pipelines – low power design – programmable DSPs – DSP architectural features/alternatives for high performance and low power.

TOTAL: 45 PERIODS

OUTCOMES:

- To be able to design architectures for DSP algorithms.
- To be able to optimize design in terms of area, speed and power.
- To be able to incorporate pipeline based architectures in the design.
- To be able to carry out HDL simulation of various DSP algorithms.

REFERENCES:

1. Keshab K.Parhi, “VLSI Digital Signal Processing Systems, Design and Implementation”, John Wiley, Indian Reprint, 2007
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, Second Edition, Indian Reprint, 2007.
3. S.Y.Kuang, H.J. White house, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1995.

AL16016	DATA CONVERTERS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To study the A/D and D/A architectures
- To study the importance of sample and hold circuits in A/D and D/A conversion techniques.

UNIT I SAMPLE AND HOLD CIRCUITS 9

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.

UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS 9

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

UNIT III DIGITAL TO ANALOG CONVERSION 9

Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.

UNIT IV ANALOG TO DIGITAL CONVERSION 9

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V PRECISION TECHNIQUES 9

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

TOTAL: 45 PERIODS

OUTCOMES:

- Explain sample and hold circuits
- Design ADC/DAC circuits
- Analyze ADC/DAC Architecture and Performance
- Discuss calibration techniques

REFERENCES:

1. Behzad Razavi, “Principles of data conversion system design”, S. Chand and company Ltd, 2000.

AL16017 SOLID STATE DEVICE MODELING AND SIMULATION

L	T	P	C
3	0	0	3

OBJECTIVES:

- To acquaint the students with fundamentals of building device and circuit simulators, and efficient use of simulators.

UNIT I MOSFET DEVICE PHYSICS **9**

MOSFET capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II DEVICE MODELLING **9**

Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. Solution of network equations: Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

UNIT III MULTISTEP METHODS **9**

Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

UNIT IV MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS **9**

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

UNIT V SIMULATION OF DEVICES **9**

Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

TOTAL: 45 PERIODS

OUTCOMES: The student who completes this course will be in a position understand the procedures used to construct the complicated device models that are widely used in VLSI CAD tools. As the CMOS technology progresses, the student will be in a position to understand the changes introduced in the device models as well as contribute to the development of appropriate device models.

REFERENCES:

1. Arora, N., “MOSFET Models for VLSI Circuit Simulation”, Springer-Verlag, 1993.
2. Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag., 1984.
3. Fjeldly, T., Yetterdal, T. and Shur, M., “Introduction to Device Modeling and Circuit Simulation”, Wiley-Interscience., 1997.
4. Grasser, T., “Advanced Device Modeling and Simulation”, World Scientific Publishing Company., 2003.
5. Chua, L.O. and Lin, P.M., “Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques”, Prentice-Hall., 1975.

6. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd.

NW16015	HIGH PERFORMANCE NETWORKS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To develop a comprehensive understanding of multimedia networking
- To study the types of VPN and tunneling protocols for security.
- To learn about network security in many layers and network management.

UNIT I INTRODUCTION 9

Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing. SONET – DWDM – DSL – ISDN – BISDN, ATM.

UNIT II MULTIMEDIA NETWORKING APPLICATIONS 9

Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.

UNIT III ADVANCED NETWORKS CONCEPTS 9

VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN. MPLS operation, Routing, Tunneling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks-P2P connections.

UNIT IV TRAFFIC MODELLING 9

Little's theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models, Network performance evaluation.

UNIT V NETWORK SECURITY AND MANAGEMENT 9

Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1

TOTAL: 45 PERIODS

OUTCOMES: Student will be able to

- Able to identify the multimedia networks around and Virtual Private Network.
- Will be able to analyze the various parameters of networking and traffic modeling of networks.
- Will be able to understand various algorithms in network security and network management involved in internet.

REFERENCES:

1. J.F. Kurose & K.W. Ross, "Computer Networking- A top down approach featuring the internet", Pearson, 2nd edition, 2003.
2. Walrand .J. Varatya, High performance communication network, Morgan Kauffman – Harcourt Asia Pvt. Ltd. 2nd Edition, 2000.
3. LEOM-GarCIA, WIDJAJA, "Communication networks", TMH seventh reprint 2002.
4. Aunurag kumar, D. MAnjunath, Joy kuri, "Communication Networking", Morgan Kaufmann Publishers, 1ed 2004.

5. Hersent Gurle & petit, “IP Telephony, packet Pored Multimedia communication Systems”, Pearson education 2003.
6. Fred Halsall and Lingana Gouda Kulkarni,” Computer Networking and the Internet” fifth edition, Pearson education 2006.
7. Nader F.Mir , Computer and Communication Networks, first edition 2010.
8. Larry l.Peterson & Bruce S.David, “Computer Networks: A System Approach”-1996.

ELECTIVE V

AL16018	TESTING OF VLSI CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To know the various types of faults and also to study about fault detection, dominance
- To know the concepts of the test generation methods-DFT-BIST.
- To understand the fault diagnosis methods.

UNIT I TESTING AND FAULT MODELLING 9

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION 9

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS 9

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon completion of the course, students will be able to

- Design a better yield in IC design
- Analyze the various test generation methods for combinational and sequential circuits. Identify the design for testability methods for combinational and sequential circuits.
- Recognize the BIST techniques for improving testability.

REFERENCES:

1. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House,2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.

AL16019 VLSI FOR WIRELESS COMMUNICATION L T P C
3 0 0 3

OBJECTIVES:

- To study the design concepts of low noise amplifiers.
- To study the various types of mixers designed for wireless communication.
- To study and design PLL and VCO.
- To understand the concepts of CDMA in wireless communication.

UNIT I COMPONENTS AND DEVICES 9

Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers.

UNIT II MIXERS 9

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion - Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case – Noise – A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT III FREQUENCY SYNTHESIZERS 9

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators -Phase Noise - A Complete Synthesizer Design Example (DECT Application).

UNIT IV SUB SYSTEMS 9

Data converters in communications, adaptive Filters, equalizers and transceivers.

UNIT V IMPLEMENTATIONS 9

VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon completion of the course, students will be able to
Design low noise amplifiers.
Analyze various types of mixers for wireless communication.
Design VLSI architecture of PLL ,VCO, CDMA in wireless communication.

REFERENCES:

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998.
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
3. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003.
4. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design - Circuits and

Systems", Kluwer Academic Publishers, 2000.
5. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999.
6. J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, Kluwer Academic Pub., 1997.

AL16020	PHOTONICS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To gain knowledge about light and its propagation.
- To study the different types of laser and its effects.
- To learn about holography.
- To study the non-linear optic devices.

UNIT I INTRODUCTION TO PHOTONICS 9

Nature of Light – Wave and light terminology, Maxwell equation, light spectra and sources, absorption and emission, black body radiation. Geometric Optics – Light as a ray, law of reflection including plane mirrors, law of refraction including optical fiber applications, prisms and thin lenses including Lensmaker's equation, Lens problems and optical instruments using the thin lens equation.

UNIT II WAVE OPTICS 9

Wave descriptive terminology, wave superposition (interference) including double – slit interference, diffraction and diffraction gratings, interference applications, eg. Michelson, Mach Zender and Fabry Perot interferometers, Thin film interference and Fiber Bragg Gratings. Diffraction Effects including: airy disk, near far field effects. Polarization principles including scattering, reflection and birefringence.

UNIT III LASERS 9

Introduction to Lasers – Basic terminology and theory of operation including specific requirements, principal types of lasers. Laser radiation hazards including effects on the eye and skin. Laser safety standards and hazard classifications. Laser safety precautions and protective measures.

UNIT IV HOLOGRAPHY 9

Holography – Theory and basic principles, Requirement to record and reconstruct holograms – Experimental techniques- Recording Materials-Reflection holography and applications-Holographic interoferrometry-Nondestructive testing, optical memory.

UNIT V NON-LINEAR OPTICS 9

Non-linear optics – Harmonic Generation, sum and difference frequency generation, wave mixing, Optical Parametric Oscillator. Non-linear optic materials – inorganic and organic. Phase matching, efficiency of harmonic generation- powder and single crystal methods. Methods of determination of harmonic coefficients – Z-scan and Electrical Field Induced Second Harmonic. Phase conjugation-Silicon Photonics-Silicon on Insulator Photonics-Fabrication of Silicon Waveguides.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon completion of the course, students will be able to

- Apply wave optics and diffraction theory to a range of problems
- Analyze mechanism of operation of Laser Emission, Absorption and Radiation
  Develop methods to apply holography in various applications.
- Analyze mechanism of nonlinear optics and origin of optical nonlinearities. They will also analyze

various types of nonlinearities in optics.

- Apply in depth knowledge of modern photonics, optical communications systems, and knowledge of photonics in technology.

REFERENCES:

1. Bahaa E. A. Saleh, Malvin Carl Teich, "Fundamentals of Photonics", John Wiley & Sons 2011.
2. T.P. Pearsall, "Photonics Essentials: An introduction with experiments", McGraw Hill 2003.
3. F.G. Smit and T.A. King, "Optics and Photonics: An introduction", Wiley & Sons, Ltd 2003.
4. B. Balkrishna Laud, "Lasers and Non-Linear Optics", New Age International 2011.
5. R.S. Quimby, "Photonics and Lasers-An Introduction", Wiley 2006.
6. R. Menzel, "Photonics", Springer-Verlag 2007
7. F.A. Jenkins and H.E. White, "Fundamentals of Optics", McGraw Hill 1976
8. Yariv Yeh and Pochi Yeh, "Photonics – Optical Electronics in Modern Communications", 6th Eition, Oxford University Press 2012.
9. Abdul Al-Azzawi, "Photonics: Principles and Practices", CRC Press 2007.
10. Graham T. Reed, Andrew P. Knights, "Silicon Photonics: An Introduction", John Wiley & Sons 2004.

AL16021 **NANO ELECTRONICS** **L T P C**
3 0 0 3

OBJECTIVES:

- To learn and understand basic concepts of Nano electronics.
- To know the techniques of fabrication and measurement.
- To gain knowledge about Nanostructure devices and logic devices.

UNIT I INTRODUCTION TO NANOELECTRONICS 9

Microelectronics towards biomolecule electronics-Particles and waves- Wave-particle duality-Wave mechanics- Schrödinger wave equation- Wave mechanics of particles: - Atoms and atomic orbitals- Materials for nanoelectronics- Semiconductors- Crystal lattices: Bonding in crystals-Electron energy bands- Semiconductor heterostructures- Lattice-matched and pseudomorphic heterostructures- Inorganic-organic heterostructures- Carbon nanomaterials: nanotubes and fullerenes.

UNIT II FABRICATION AND MEASUREMENT TECHNIQUES 9

Growth, fabrication, and measurement techniques for nanostructures- Bulk crystal and heterostructure growth- Nanolithography, etching, and other means for fabrication of nanostructures and nanodevices- Techniques for characterization of nanostructures-Spontaneous formation and ordering of nanostructures- Clusters and nanocrystals- Methods of nanotube growth- Chemical and biological methods for nanoscale fabrication- Fabrication of nano-electromechanical systems.

UNIT III PROPERTIES 9

Dielectrics-Ferroelectrics-Electronic Properties and Quantum Effects-Magnetoelectronics – Magnetism and Magnetotransport in Layered Structures-Organic Molecules – Electronic Structures, Properties, and Reactions-Neurons – The Molecular Basis of their Electrical Excitability-Circuit and System Design- Analysis by Diffraction and Fluorescence Methods-Scanning Probe Techniques.

UNIT IV NANO STRUCTURE DEVICES 9

Electron transport in semiconductors and nanostructures- Time and length scales of the electrons in solids- Statistics of the electrons in solids and nanostructures- Density of states of electrons in nanostructures- Electron transport in nanostructures-Electrons in traditional low dimensional structures- Electrons in quantum wells- Electrons in quantum wires-Electrons in quantum dots-Nanostructure devices- Resonant-tunneling diodes- Field-effect transistors- Single-electron-transfer devices- Potential-effect transistors- Light-emitting diodes and lasers- Nano-electromechanical system devices- Quantum-dot cellular automata.

UNIT V LOGIC DEVICES AND APPLICATIONS 9

Logic Devices-Silicon MOSFETs-Ferroelectric Field Effect Transistors-Quantum Transport Devices Based on Resonant Tunneling-Single-Electron Devices for Logic Applications-Superconductor Digital Electronics-Quantum Computing Using Superconductors-Carbon Nanotubes for Data Processing-Molecular Electronics.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon completion of the course, students will be able to:

- Have a good understanding in Nano Electronics.
- Have a clear understanding of different fabrication and measurement techniques of Nanostructrure and logic devices.

REFERENCES:

1. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications", Cambridge University Press 2011.
2. Supriyo Datta,"Lessons from Nanoelectronics: A New Perspective on Transport", World Scientific 2012.
3. George W. Hanson,"Fundamentals of Nanoelectronics", Pearson 2009.
4. Korkin, Anatoli; Rosei, Federico (Eds.), "Nanoelectronics and Photonics",Springer 2008.
5. Mircea Dragoman, Daniela Dragoman, "Nanoelectronics: principles and devices", CRC Press 2006.
6. Karl Goser, Peter Glösekötter, Jan Dienstuhl,"Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices", Springer 2004.
7. W. R. Fahrner, Nanotechnology and Nan electronics: Materials, Devices, Measurement Techniques (SpringerVerlag Berlin Heidelberg 2005).
8. Mark A. Reed, Takhee Lee,"Molecular nanoelectronics", American Scientific Publishers 2003.
9. Jaap Hoekstra, "Introduction to Nanoelectronic Single-Electron Circuit Design", Pan Stanford Publishing 2010.
10. W. Ranier, "Nano Electronics and Information Technology", John Wiley & Sons 2012.

AL16022 **PATTERN RECOGNITION** **L T P C**
3 0 0 3

OBJECTIVES:

- To know about Supervised and unsupervised Learning.
- To study about feature extraction and structural pattern recognition.
- To explore different classification models.
- To understand Fuzzy Pattern Classifiers and Perception.

UNIT I PATTERN CLASSIFIER **9**

Overview of Pattern recognition – Discriminant functions – Supervised learning – Parametric estimation – Maximum Likelihood Estimation – Bayesian parameter
Estimation – Problems with Bayes approach– Pattern classification by distance functions – Minimum distance pattern classifier.

UNIT II CLUSTERING **9**

Clustering for unsupervised learning and classification – Clustering concept – C Means algorithm – Hierarchical clustering – Graph theoretic approach to pattern Clustering – Validity of Clusters.

UNIT III FEATURE EXTRACTION AND STRUCTURAL PATTERN RECOGNITION **9**

KL Transforms – Feature selection through functional approximation – Binary selection -Elements of formal grammars - Syntactic description - Stochastic grammars - Structural representation.

UNIT IV HIDDEN MARKOV MODELS AND SUPPORT VECTOR MACHINE **9**

State Machines – Hidden Markov Models – Training – Classification – Support vector Machine – Feature Selection.

UNIT V RECENT ADVANCES **9**

Fuzzy logic – Fuzzy Pattern Classifiers – Pattern Classification using Genetic Algorithms – Case Study Using Fuzzy Pattern Classifiers and Perception.

TOTAL: 45 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to

- Classify the data and identify the patterns.
- Extract feature set and select the features from given data set.

REFERENCES:

1. M. Narasimha Murthy and V. Susheela Devi, “Pattern Recognition”, Springer 2011.
2. S.Theodoridis and K.Koutroumbas, “Pattern Recognition”, 4th Ed., Academic Press, 2009.
3. Robert J.Schalkoff, “Pattern Recognition Statistical, Structural and Neural Approaches”, John Wiley & Sons Inc., New York, 1992.
4. C.M.Bishop, “Pattern Recognition and Machine Learning”, Springer, 2006.
5. R.O.Duda, P.E.Hart and D.G.Stork, “Pattern Classification”, John Wiley, 2001.

6. Andrew Webb, “Stastical Pattern Recognition”, Arnold publishers, London,1999.

CU16017 **OPTICAL COMPUTING** **L T P C**
3 0 0 3

OBJECTIVES:

- To know the basic pricinciples of optical computing.
- To study about various optical computing elements.
- To study and compare analog and digital optical computing.

UNIT I OPTICAL COMPUTING PRINCIPLES 9

Non Von-Neuman architecture, various forms of parallel processing, SLM, LEDs, Lasers and Photo detectors arrays, Holographic techniques, Optical storage devices.

UNIT II DIGITAL LOGIC 9

Symbolic substitution, Image computing, Cellular logic, Boolean logic, Cellular arrays, Cellular hyper cubes, conventional hyper cube, Binary stack coded arithmetic, Binary Row coded, Binary symbol, Coded arithmetic multilevel logic processing.

UNIT III OPTICAL COMPUTING ELEMENTS 9

ß switches, Machzender interferometeric logic elements for Boolean functions, Acousto optic; optical matrix multipliers, Nonlinear optical switches as memories.

UNIT IV ANALOG OPTICAL COMPUTING 9

Linear optic processing, Analog optical arithmatics. Recognition by analog optical system.

UNIT V DIGITAL OPTICAL COMPUTING 9

Devices, Shadow casting, Symbolic substitution, Optical matrix processing, Optical linear neural network. Nonlinear network.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon Completion of the course, the students will be able to

- To adopt new technology for a future computer
- Understand new concept and basic knowledge of computing using optical wave instead of electron in transistors.
- Analyze massive parallel processing and fault-tolerant computing.
  Understand various optical computing elements.
- Learn an optical sequential computing machine

REFERENCES:

1. A.Karim Mohammed and A.S.Abdul Awwall, Optical computing-An introduction, John Wiley, New York, 1992.
2. Mc. Aulay Alastair.D, Optical Computer Architecture: The Application of optical concepts to next generation computers, John Wiley, New York, 1991.
3. Dror Feitelsen, Optical Computing, MIT press, Cambridge, 1988.

ELECTIVE VI

AL16026	ROBOTICS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand robot locomotion and mobile robot kinematics.
- To understand perception in robotics.
- To understand mobile robot localization.
- To understand mobile robot mapping.
- To understand simultaneous localization and mapping (SLAM).
- To understand robot planning and navigation.

UNIT I LOCOMOTION AND KINEMATICS 9

Introduction to Robotics – key issues in robot locomotion – legged robots – wheeled mobile robots – aerial mobile robots – introduction to kinematics – kinematics models and constraints – robot maneuverability.

UNIT II ROBOT PERCEPTION 9

Sensors for mobile robots – vision for robotics – cameras – image formation – structure from stereo – structure from motion – optical flow – color tracking – place recognition – range data.

UNIT III MOBILE ROBOT LOCALIZATION 9

Introduction to localization – challenges in localization – localization and navigation – belief representation – map representation – probabilistic map-based localization – Markov localization – EKF localization – UKF localization – Grid localization – Monte Carlo localization – localization in dynamic environments.

UNIT IV MOBILE ROBOT MAPPING 9

Autonomous map building – occupancy grip mapping – MAP occupancy mapping – SLAM – extended Kalman Filter SLAM – graph-based SLAM – particle filter SLAM – sparse extended information filter – fastSLAM algorithm.

UNIT V PLANNING AND NAVIGATION 9

Introduction to planning and navigation – planning and reacting – path planning – obstacle avoidance techniques – navigation architectures – basic exploration algorithms.

TOTAL: 45 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to

- Explain robot locomotion.
- Apply kinematics models and constraints.
- Implement vision algorithms for robotics.
- Implement robot localization techniques.
- Implement robot mapping techniques.
- Implement SLAM algorithms.

- Explain planning and navigation in robotics.

REFERENCES:

1. Roland Seigwart, Illah Reza Nourbakhsh, and Davide Scaramuzza, "Introduction to autonomous mobile robots", Second Edition, MIT Press, 2011.
2. Sebastian Thrun, Wolfram Burgard, and Dieter Fox, "Probabilistic Robotics", MIT Press, 2005.
3. Howie Choset et al., "Principles of Robot Motion: Theory, Algorithms, and Implementations", A Bradford Book, 2005.
4. Gregory Dudek and Michael Jenkin, "Computational Principles of Mobile Robotics", Second Edition, Cambridge University Press, 2010.
5. Maja J. Mataric, "The Robotics Primer", MIT Press, 2007.

CU16018 OPTICAL IMAGING TECHNIQUES

L	T	P	C
3	0	0	3

OBJECTIVES:

- To learn the fundamentals of optical image formation and fourier optics.
- To study and compare coherent and incoherent optical imaging.
- To know the various techniques in the construction of image.

UNIT I FUNDAMENTALS **9**

Coherance and light source – optical image formation – Franhoufer diffraction – Single slit – double slit circular aperture – double aperture gratings – 1D and 2D lens aperture – Interference.

UNIT II FOURIER SERIES AND TRANSFORM **9**

Fourier series – Fourier coefficients – optical and crystal diffraction gratings – Fourier series formulation – Fourier transform and single slit diffraction – grating pattern – Fourier transform of light waves – correlation.

UNIT III OPTICAL IMAGING AND PROCESSING **9**

Incoherent optical imaging – transfer function – coherent optical imaging – periodic and non-periodic objects – optical transform – Holography – coherent and incoherent optical processing.

UNIT IV IMAGE CONSTRUCTION TECHNIQUES **9**

X – ray computed tomography – reconstruction by simple back projection – iterative reconstruction – analysis methods – magnetic resonance imaging – Ultrasonic computed tomography.

UNIT V APPLICATIONS **9**

Michelsons stellar interferometry – spectral interferometer – fringe visibility and spectral distribution – partial coherence and correlation – Fourier transform spectroscopy – Synthetic aperture radar – Intensity interferometer – Imaging by holographic techniques.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon Completion of the course, the students will be able to

- Develop understanding of basic optics and concepts in optical imaging, Fourier imaging Analyze number of important technologies based on diffractive wave propagation
- Acquire knowledge of developments in the areas of optical image processing. Deal with image reconstruction techniques
- Acquire knowledge of applications in the areas of optical imaging.

REFERENCES:

1. E.G. Stewart, “Fourier Optics an Introduction”, 2nd Edition, Ellis Harwood limited, Chichester, 1987.
2. Dror.G. Feitelson, “Optical Computing”, MIT press, Cambridge, 1988.

AL16023	MEMS AND NEMS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introducing the concepts of microelectromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To introducing concepts of quantum mechanics and nano systems.

UNIT I OVERVIEW AND INTRODUCTION 9

New trends in Engineering and Science: Micro and Nanoscale systems Introduction to Design of MEMS and NEMS, Overview of Nano and Microelectromechanical Systems, Applications of Micro and Nanoelectromechanical systems, Microelectromechanical systems, devices and structures Definitions, Materials for MEMS: Silicon, silicon compounds, polymers, metals.

UNIT II MEMS FABRICATION TECHNOLOGIES 9

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials.

UNIT III MICRO SENSORS 9

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT IV MICRO ACTUATORS 9

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS 9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wavefunction Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon Completion of the course, the students will be able to

- Identify the scope and applications of Micro and Nanoelectromechanical systems
- Design of fabrication techniques used in MEMS
- Identify various micro sensors used in MEMS
- Identify the Micro actuators which can be used in MEMS and to apply them suitably.
- Design different types of MEMS/NEMS devices depending on the required application

REFERENCES:

1. Marc Madou, “Fundamentals of Microfabrication”, CRC press 1997.

2. Stephen D. Senturia," Micro system Design", Kluwer Academic Publishers,2001.
3. Tai Ran Hsu ,"MEMS and Microsystems Design and Manufacture" ,Tata Mcraw Hill, 2002.
4. Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006.
5. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002.

CU16004 SPEECH AND AUDIO SIGNAL PROCESSING

L	T	P	C
3	0	0	3

OBJECTIVES:

- To study the basic concepts of speech and audio.
- To study the analysis of various M-band filter banks for audio coding.
- To learn various transform coders for audio coding.
- To study the speech processing methods in time and frequency domain.

UNIT I MECHANICS OF SPEECH AND AUDIO 9

Introduction - Review of Signal Processing Theory-Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Absolute Threshold of Hearing - Critical Bands- Simultaneous Masking, Masking-Asymmetry, and the Spread of Masking- Nonsimultaneous Masking - Perceptual Entropy - Basic measuring philosophy -Subjective versus objective perceptual testing - The perceptual audio quality measure (PAQM) - Cognitive effects in judging audio quality.

UNIT II TIME-FREQUENCY ANALYSIS: FILTER BANKS AND TRANSFORMS 9

Introduction -Analysis-Synthesis Framework for M-band Filter Banks- Filter Banks for Audio Coding: Design Considerations - Quadrature Mirror and Conjugate Quadrature Filters- Tree-Structured QMF and CQF M-band Banks - Cosine Modulated "Pseudo QMF" M-band Banks - Cosine Modulated Perfect Reconstruction (PR) M-band Banks and the Modified Discrete Cosine Transform (MDCT) - Discrete Fourier and Discrete Cosine Transform - Pre-echo Distortion- Pre echo Control Strategies.

UNIT III AUDIO CODING AND TRANSFORM CODERS 9

Lossless Audio Coding-Lossy Audio Coding- ISO-MPEG-1A,2A,2A Advanced , 4A Audio Coding -Optimum Coding in the Frequency Domain - Perceptual Transform Coder -Brandenburg-Johnston Hybrid Coder - CNET Coders - Adaptive Spectral Entropy Coding -Differential Perceptual Audio Coder - DFT Noise Substitution -DCT with Vector Quantization -MDCT with Vector Quantization.

UNIT IV TIME AND FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING 9

Time domain parameters of Speech signal – Methods for extracting the parameters: Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy Short Time Fourier analysis – Formant extraction – Pitch Extraction using time and frequency domain methods. **HOMOMORPHIC SPEECH ANALYSIS**: Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders.

UNIT V LINEAR PREDICTIVE ANALYSIS OF SPEECH 9

Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin's Recursive algorithm – lattice formation and solutions – Comparison of different methods –

Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon Completion of the course, the students will be able to

- Understand the fundamentals of audio and speech signal processing and associated techniques.
- Understand how to solve practical problems with some basic audio & speech signal processing techniques.
- Analyze and design algorithms to extract parameters from the speech signal.
- Analyze and design algorithms for coding speech and audio signal.

REFERENCES:

1. Digital Audio Signal Processing, Second Edition, Udo Zölzer, A John Wiley& sons Ltd Publications.
2. Applications of Digital Signal Processing to Audio And Acoustics Mark Kahrs, Karlheinz Brandenburg, Kluwer academic publishers New York, Boston, Dordrecht, London , Moscow.
3. Digital Processing of Speech signals – L.R.Rabiner and R.W.Schaffer - Prentice Hall – 1978.

AL16024 **SYSTEM ON CHIP DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- To design combinational and sequential logic networks.
- To learn optimization of power in combinational and sequential logic machines.
- To study the design principles of FPGA and PLA.
- To learn various floor planning methods for system design.

UNIT I LOGIC GATES 9

Introduction. Combinational Logic Functions. Static Complementary Gates. Switch Logic. Alternative Gate Circuits. Low-Power Gates. Delay Through Resistive Interconnect. Delay Through Inductive Interconnect.

UNIT II COMBINATIONAL LOGIC NETWORKS 9

Introduction. Standard Cell-Based Layout. Simulation. Combinational Network Delay. Logic and interconnect Design. Power Optimization. Switch Logic Networks. Combinational Logic Testing.

UNIT III SEQUENTIAL MACHINES 9

Introduction. Latches and Flip-Flops. Sequential Systems and Clocking Disciplines. Sequential System Design. Power Optimization. Design Validation. Sequential Testing.

UNIT IV SUBSYSTEM DESIGN 9

Introduction. Subsystem Design Principles. Combinational Shifters. Adders. ALUs. Multipliers. High-Density Memory. Field Programmable Gate Arrays. Programmable Logic Arrays. References. Problems.

UNIT V FLOOR-PLANNING 9

Introduction, Floor-planning Methods – Block Placement & Channel Definition, Global Routing, switchbox Routing, Power Distribution, Clock Distributions, Floor-planning Tips, Design Validation. Off-Chip Connections – Packages, The I/O Architecture, PAD Design.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon Completion of the course, the students will be able to

- Identify suitable logics gates used in SOC
- Design combinational and sequential logic networks for SOC
- Optimize power in logic design.
- Implement FPGA and PLA for subsystem design.
- Apply suitable floor planning techniques to optimise the performance of SOC

REFERENCES:

1. Wayne Wolf, "Modern VLSI Design – System – on – Chip Design", Prentice Hall, 3rd Edition 2008.
2. Wayne Wolf , " Modern VLSI Design – IP based Design", Prentice Hall, 4th Edition , 2008.

CP16035	RECONFIGURABLE COMPUTING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the need for reconfigurable computing.
- To expose the students to various device architectures.
- To examine the various reconfigurable computing systems.
- To understand the different types of compute models for programming reconfigurable architectures.
- To expose the students to HDL programming and familiarize with the development environment.
- To expose the students to the various placement and routing protocols.
- To develop applications with FPGAs.

UNIT I DEVICE ARCHITECTURE 9

General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices – Complex Programmable Logic Devices – FPGAs – Device Architecture - Case Studies.

UNIT II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS 9

Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Case Studies – Reconfiguration Management.

UNIT III PROGRAMMING RECONFIGURABLE SYSTEMS 9

Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing.

UNIT IV MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS 9

The Design Flow - Technology Mapping – FPGA Placement and Routing – Configuration Bitstream Generation – Case Studies with Appropriate Tools.

UNIT V APPLICATION DEVELOPMENT WITH FPGAS 9

Case Studies of FPGA Applications – System on a Programmable Chip (SoPC) Designs.

TOTAL: 45 PERIODS

OUTCOMES:

Upon completion of the course, the students will be able to

- Identify the need for reconfigurable architectures.
- Discuss the architecture of FPGAs.
- Point out the salient features of different reconfigurable architectures.
- Build basic modules using any HDL.
- Develop applications using any HDL and appropriate tools.
- Design and build an SoPC for a particular application.

REFERENCES:

1. Maya B. Gokhale and Paul S. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.
2. Scott Hauck and Andre Dehon (Eds.), "Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation", Elsevier / Morgan Kaufmann, 2008.
3. Christophe Bobda, "Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications", Springer, 2010.

NW16016 WIRELESS ADHOC AND SENSOR NETWORKS L T P C
3 0 0 3

COURSE OBJECTIVES:

- To know the constraints of the wireless physical layer that affect the design and performance
  of ad hoc and sensor networks, protocols, and applications.
- To understand MAC, Routing protocols that have been proposed for ad hoc and sensor networks
- To understand the energy issues in sensor networks and how they can be addressed using scheduling, media access control, and special hardware
- To explain various security threats to ad hoc networks and describe proposed solutions

UNIT I ADHOC NETWORKS AND ROUTING PROTOCOLS 9

Ad hoc Wireless Networks – What is an Ad Hoc Network? Heterogeneity in Mobile Devices – Wireless Sensor Networks – Traffic Profiles – Types of Ad hoc Mobile Communications – Types of Mobile Host Movements – Challenges Facing Ad hoc Mobile Networks – Ad hoc wireless Internet. Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks – Classifications of Routing Protocols – Table–Driven Routing Protocols – Destination Sequenced Distance Vector (DSDV) – Wireless Routing Protocol (WRP) – Cluster Switch Gateway Routing (CSGR) – Source–Initiated On–Demand Approaches – Ad hoc On– Demand Distance Vector Routing(AODV) – Dynamic Source Routing (DSR) –Temporally Ordered Routing Algorithm (TORA) –Signal Stability Routing (SSR) –Location–Aided Routing (LAR) – Power–Aware Routing (PAR) –Zone Routing Protocol (ZRP).

UNIT II MULTICAST ROUTING AND SECURITY 9

Issues in Designing a Multicast Routing Protocol – Operation of Multicast Routing Protocols –An Architecture Reference Model for Multicast Routing Protocols –Classifications of Multicast Routing Protocols – Tree–Based Multicast Routing Protocols– Mesh–Based Multicast Routing Protocols – Summary of Tree and Mesh based Protocols – Energy– Efficient Multicasting – Multicasting with Quality of Service Guarantees – Application – Dependent Multicast Routing – Comparisons of Multicast Routing Protocols - Design Goals of a Transport Layer Protocol for Ad hoc Wireless Networks –Classification of Transport Layer Solutions – TCP over Ad hoc Wireless Networks- Security in Ad Hoc Wireless Networks – Network Security Requirements – Issues and Challenges in Security Provisioning – Network Security Attacks – Key Management – Secure Routing in Ad hoc Wireless Networks.

UNIT III QoS AND ENERGY MANAGEMENT 9

Issues and Challenges in Providing QoS in Ad hoc Wireless Networks – Classifications of QoS Solutions – MAC Layer Solutions – Network Layer Solutions – QoS Frameworks for Ad hoc Wireless Networks Energy Management in Ad hoc Wireless Networks – Introduction – Need for Energy Management in Ad hoc Wireless Networks – Classification of Energy Management Schemes – Battery Management Schemes – Transmission Power Management Schemes –System Power Management Schemes.

UNIT IV SENSOR NETWORKS – ARCHITECTURE AND MACPROTOCOLS 9

Single node architecture – Hardware components, energy consumption of sensor nodes, Network architecture – Sensor network scenarios, types of sources and sinks, single hop versus multi-hop networks, multiple sinks and sources, design principles, Development of wireless sensor networks, physical layer and transceiver design consideration in wireless sensor networks, Energy usage profile, choice of modulation, Power Management - MAC protocols –fundamentals of wireless MAC protocols, low duty cycle protocols and wakeup concepts, contention-based protocols, Schedule-based protocols - SMAC, BMAC, Traffic-adaptive medium access protocol (TRAMA), Link Layer protocols – fundamentals task and requirements ,error control, framing, link management.

UNIT V SENSOR NETWORKS – ROUTING PROTOCOLS AND OPERATING SYSTEMS 9

Gossiping and agent-based uni-cast forwarding, Energy-efficient unicast, Broadcast and multicast, geographic routing, mobile nodes, Data-centric routing – SPIN, Directed Diffusion, Energy aware routing, Gradient-based routing – COUGAR, ACQUIRE, Hierarchical Routing –LEACH, PEGASIS, Location Based Routing – GAF, GEAR, Data aggregation – Various aggregation techniques. Introduction to TinyOS – NesC, Interfaces, modules, configuration, Programming in TinyOS using NesC, Emulator TOSSIM.

TOTAL: 45 PERIODS

COURSE OBJECTIVES:

- To know the constraints of the wireless physical layer that affect the design and performance of ad hoc and sensor networks, protocols, and applications.
- To understand MAC, Routing protocols that have been proposed for ad hoc and sensor networks
- To understand the energy issues in sensor networks and how they can be addressed using scheduling, media access control, and special hardware
- To explain various security threats to ad hoc networks and describe proposed solutions

COURSE OUTCOMES: Upon completion of the course, the students will be able to

- Identify the unique issues and challenges in ad-hoc/sensor networks.
- Describe the current technology trends for the implementation and deployment of wireless ad-hoc/sensor networks.
- Discuss the challenges in designing MAC, routing and transport protocols for wireless ad-hoc/sensor networks.
- Comprehend the various sensor network Platforms, tools and applications

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2. C. K. Toh, “Ad Hoc Mobile Wireless Networks Protocols and Systems”, Prentice Hall, PTR,2001.
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ELECTIVE VII

CU16203	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the basics of EMI.
- To study EMI Sources.
- To understand EMI problems.
- To understand Solution methods in PCB.
- To understand Measurement technique for emission.
- To understand Measurement technique for immunity.

UNIT I EMI/EMC CONCEPTS **9**

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES **9**

Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling, cross talk; Field to cable coupling; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES **9**

Shielding- Shielding Material-Shielding integrity at discontinuities, Filtering- Characteristics of Filters-Impedance and Lumped Element Filters-Telephone line filter, Power line filter design, Filter installation and Evaluation, Grounding- Measurement of Ground resistance-system grounding for EMI/EMC-Cable shielded grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control. EMI gaskets.

UNIT IV EMC DESIGN OF PCBS **9**

EMI Suppression Cables-Absorptive, ribbon cables-Devices-Transient protection hybrid circuits, Component selection and mounting; PCB trace impedance; Routing; Cross talk control-Electromagnetic Pulse-Noise from relays and switches, Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS **9**

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462. Frequency assignment - spectrum conversation. British VDE standards, Euro norms standards in japan - comparisons. EN Emission and Susceptibility standards a nd Specifications.

TOTAL: 45 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to

- To design a EMI free system.
- To reduce system level crosstalk.

- To design high speed Printed Circuit board with minimum interference.
- To make our world free from unwanted electromagnetic environment.

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1. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork, 1996.
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AL16027 RECONFIGURABLE ARCHITECTURES

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To study the various classifications of Reconfigurable Computing Systems
- To study the various FPGA Technologies, FPGA Architectures, Routing strategies in FPGAs
- To study the high level design for synthesis, simulation, timing analysis and functional verification
- To study area efficient and power efficient application specific architectures

UNIT I INTRODUCTION 9

Domain-specific processors, Application specific processors, Reconfigurable Computing Systems –Evolution of reconfigurable systems –Characteristics of RCS-advantages and issues. Fundamental concepts & Design steps –classification of reconfigurable architecture-fine, coarse grain & hybrid architectures –Examples.

UNIT II FPGA TECHNOLOGIES & ARCHITECTURE 9

Technology Trends-Programming technology-SRAM programmed FPGAs, antifuse programmed FPGAs, erasable programmable logic devices. Alternative FPGA architectures: Mux Vs LUT based logic blocks –CLB Vs LAB Vs Slices-Fast carry chains-Embedded RAMs-FPGA Vs ASIC design styles.

UNIT III ROUTING FOR FPGAS 9

General Strategy for Touting in FPGAs-routing for row-based FPGAs –segmented channel routing, definitions-Algorithm for I segment and K segment routing –Routing for symmetrical FPGAs, Flexibility of FPGA Routing Architectures: FPGA architectural assumptions-logic block, connection block, switch block, -Effect of connection block flexibility on Routability-Effect of switch block flexibility on rountability - Tradeoffs in flexibility of S and C blocks

UNIT IV HIGH LEVEL DESIGN 9

FPGA Design style: Technology independent optimization-technology mapping-Placement. High-level synthesis of reconfigurable hardware, high-level languages, Design tools: Simulation (cycle based, event driven based) –Synthesis (logic/HDL vs physically aware) –timing analysis (static vs dynamic)-verification physical design tools.

UNIT V APPLICATION SPECIFIC RCS 9

RCS for FFT algorithms-area efficient architectures-power efficient architectures-low energy reconfigurable single chip DSP system-minimizing the memory requirement for continuous flow FFT implementation-memory reduction methods for FFT implementation RCS for Embedded cores, image processing.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon Completion of the course, the students will be able to

- Design a EMI free system
- Reduce system level crosstalk
- Design high speed Printed Circuit board with minimum interference Make our world free from unwanted electromagnetic environment

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AL16028 MULTIPROCESSOR INTERCONNECTION NETWORKS

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To understand the classification, architecture and switching techniques of interconnection networks
- To study the deterministic and adaptive routing algorithms
- To study the issues related to the area, energy, reliability and quality of service of Network on Chip (NoC)
- To analyze the performance issues in analytical and simulation approaches

UNIT I ICN ARCHITECTURES **9**

Introduction –Classification of ICNs -Topologies -Direct Networks -Indirect Networks.

UNIT II SWITCHING TECHNIQUES **9**

Basic switching techniques -Virtual channels –Hybrid switching techniques Optimizing switching techniques -Comparison of switching techniques -Deadlock, livelock and Starvation Issues.

UNIT III ROUTING ALGORITHMS **9**

Taxonomy of routing algorithms -deterministic routing algorithms -Partially adaptive algorithms -Fully adaptive algorithms -Routing in MINs -Routing in switch-based networks with irregular topologies -Resource allocation policies.

UNIT IV NETWORK-ON-CHIP **9**

NoC Architectures -Area, energy and reliability constraints -NoC design alternatives -Quality-of Service (QoS) issues in NoC architectures.

UNIT V PERFORMANCE ANALYSIS **9**

Performance issues –Analytical and Simulation approaches –Fault-tolerance issues –Case studies.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon Completion of the course, the students will be able to

- Characterize Reversible Computing Systems and choose the domain or application specific processors
- Choose the Architecture, Technologies and Routing strategies for an application
- Use high level languages and hardware description languages for design, synthesize, simulate and verify reconfigurable hardware.
- Design area efficient and power efficient application specific Reversible Computing Systems

REFERENCES:

1. William J. Dally and Brian Towels, "Principles and Practices of Interconnection Networks", ISBN: 0122007514, Morgan Kaufmann, 2003.
2. Giovanni Deicheli, Luca Benini, "Networks on Chips: Technology and Tools", ISBN: 0123705215, Morgan Kaufmann, 2006.
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AL16029	MIXED SIGNAL VLSI DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To understand the basic analog building blocks, active and switched capacitor filters
- To study the design and implementation of continuous time and digital filters
- To uderstand ADC, DAC and Sigma-Delta converters
- To study about the mixed layout VLSI issues

UNIT I BASIC ANALOG BUILDING BLOCKS 9

Current mirrors – Voltage sources/references – Voltage amplifiers – Transconductance and Transresistance amplifiers – Operational amplifiers – Comparators – Multipliers.

UNIT II INTRODUCTION TO ACTIVE FILTERS AND SWITCHED CAPACITOR FILTERS 9

Active RC Filters for monolithic filer design : First and Second order filter realizations - Universal active filter (KHN) – Self tuned filter – Programmable filters – Switched capacitor filters: Switched capacitor resistors – amplifiers – comparators – sample and hold circuits – Integrator – BiQuad.

UNIT III CONTINUOUS TIME FILTERS AND DIGITAL FILTERS 9

Introduction to Gm - C filters – bipolar transconductors – CMOS Transconductors using Triode transistors, active transistors – BiCMOS transconductors – MOSFET C Filters – Tuning Circuitry – Dynamic range performance – Digital Filters: Sampling - decimation – Interpolation – Implementation of FIR and IIR filters.

UNIT IV DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTERS 9

Non-idealities in the DAC – Types of DACs: Current switched, Resistive, Charge redistribution (capacitive), Hybrid, segmented DACs – Techniques for improving linearity – Analog to Digital Converters: quantization errors – non-idealities – types of ADCs: Flash, two step, pipelined, successive approximation, folding ADCs.

UNIT V SIGMA DELTA CONVERTERS 9

Over sampled converters – Over sampling without noise and with noise – Implementation imperfections – First order modulator – Decimation filters – Second order modulator – Sigma delta DAC and ADCs, Mixed Layout: CMOS design rules – Layout of CMOS – BJT – Capacitors – Resistors – Mixed layout issues: Floor planning, power supply and ground, fully differential matching, Guard rings and shielding.

TOTAL: 45 PERIODS

COURSE OUTCOMES: Upon Completion of the course, the students will be able to

- Recommend the architecture and switching techniques of interconnection networks for a given application
- Develop deterministic and adaptive routing algorithms Address the issues related to the area, energy, reliability
- Analyze the performance issues and choose the appropriate approach for the design

REFERENCES:

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NW16022	WIRELESS SECURITY	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To explore variety of attacks and threats and its impact on MAC layer and Network layer.
- To study characteristics, vulnerabilities and challenges of ad hoc networks.
- To provide solution for covering the security principles and flaws of popular wireless technologies.
- To evaluate the performance of secured routing protocols in MANETs.

UNIT I ATTACKS ON ROUTING PROTOCOLS 9

Vulnerability of MANET to attack - review of AODV and DSR - type of attack - active and passive - internal and external - behavior of malicious node - black hole, DoS, Routing table overflow, Impersonation, Energy consumption, Information Disclosure - Misuse type – Misuse goals – Security flaw in AODV -attack on AODV - wormhole and rushing attack –Performance analysis of AODV in the presence of malicious node.

UNIT II INTRUSION DETECTION IN WIRELESS AD HOC NETWORKS 9

Problem in current IDS techniques - requirements of IDS - classification of IDS – Network and host based - anamoly detection, misuse detection, specification based - intrusion detection in MANETs using distributed IDS and mobile agents - AODV protocol based IDS – Intrusion resistant routing algorithms - Comparison of IDS.

UNIT III MITIGATING TECHNIQUES FOR ROUTING MISBEHAVIOR 9

Watchdog, Parthrater, Packet leashes and RAP.

UNIT IV SECURE ROUTING PROTOCOLS 9

Self-organized network layer security in MANETs - mechanism to improve authentication and integrity in AODV using hash chain and digital signatures - on demand secure routing protocol resilent to Byzantine failures - ARIADNE, SEAD, SAR, and ARAN.

UNIT V CHALLENGES IN ROUTING SECURITY AND FUTURE RESEARCH DIRECTIONS 9

Security - Challenges and solutions - Providing Robust and Ubiquitous security support - Adaptive security for multilevel Ad Hoc Network - Denial of service Attack at the MAC layer – Detection and handling of MAC layer Misbehavior. Opportunistic routing to mitigate attacks in MANET- The Security of Vehicular Adhoc Networks- Asymmetric and dynamic encryption for routing security in MANET.

TOTAL: 45 PERIODS

OUTCOMES:

- Ability to identify the various attacks and threads of wireless Networks.
- Understand and recognize the architectures, vulnerabilities and challenges of mobile protocols.
- Analyze the solutions for covering the security principles of wireless networks.
- Analyze and design security systems for wireless networks.
- Apply in-depth knowledge of wireless communications principles, systems, and networks to the solution of wireless engineering problems.

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1. C.Siva Ram Murthy and B.S.Manoj, AdHoc Wireless Networks: Architectures and Protocols, Prentice Hall PTR, 2004.
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