SRI VENKATESWARA COLLEGE OF ENGINEERING
(An Autonomous Institution, Affiliated to Anna University, Chennai)
SRIPERUMBUDUR TK - 602 117

REGULATION – 2018
M.E. APPLIED ELECTRONICS
Choice Based Credit System
I - IV Semesters CURRICULUM

SEMESTER I

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C	Prerequisites	Fixed/Movable
THEORY										
1.	MA18181	Applied Mathematics for Engineers (Common to AL,CU and PD)	FC	4	3	1	0	4	-	F
2.	AL18101	Advanced Digital Signal Processing	PC	3	3	0	0	3	-	F
3.	AL18102	Analog Integrated Circuit Design	PC	3	3	0	0	3	-	F
4.	AL18103	Embedded Systems Design	PC	3	3	0	0	3	-	F
5.		Elective I	PE	3	3	0	0	3	-	M
PRACTICAL										
6.	AL18111	Embedded Systems Design Laboratory	PC	4	0	0	4	2	-	F
7.	CU18112	Advanced Digital Signal Processing Laboratory (Common to AL & CU)	PC	4	0	0	4	2	-	F
TOTAL				**33**	**15**	**1**	**8**	**20**	-	-

SEMESTER II

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C	Prerequisites	Fixed/Movable
THEORY										
1.	AL18201	ASIC and FPGA Design	PC	4	3	0	0	3		F
2.	AL18202	Analog and Digital CMOS VLSI Design	PC	4	3	0	0	3		F
3.		Elective II	PE	4	3	0	0	3	-	M
4.		Elective III	PE	4	3	0	0	3	-	M
5.	MC18081	Introduction to Research Methodology and IPR	MC	2	2	0	0	2	-	F
PRACTICAL										
6.	AL18211	Integrated Circuits Design Laboratory	PC	4	0	0	4	2		F
7.	AL18212	Analog and Digital CMOS VLSI Design Laboratory	PC	4	0	0	4	2		F
8.	AL18213	Mini Project	EEC	4	0	0	4	2	-	F
TOTAL				**30**	**14**	**0**	**12**	**20**	-	-

SEMESTER III

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C	Prerequisites	Fixed/Movable
THEORY										
1.		Elective IV	PE	4	3	0	0	3	-	M
2.		Elective V	PE	4	3	0	0	3	-	M
3.		Elective VI	PE	4	3	0	0	3	-	M
PRACTICAL										
4.	AL18311	Project Work Phase I	EEC	12	0	0	12	6	-	F
TOTAL				**24**	**9**	**0**	**12**	**15**	-	-

SEMESTER IV

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C	Prerequisites	Fixed/Movable
PRACTICAL										
1.	AL18411	Project Work Phase II	EEC	24	0	0	24	12	-	F
TOTAL				**24**	**0**	**0**	**24**	**12**	**-**	**-**

Total Credits: 67

PROFESSIONAL ELECTIVES (PE)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C	Prerequisites	Fixed/Movable
1.	AL18001	Internet of Things for Electronics Engineers	PE	4	3	0	0	3		
2.	AL18002	Synthesis and Optimization of Digital circuits	PE	4	3	0	0	3		
3.	AL18003	Advanced Microprocessors And Microcontrollers	PE	4	3	0	0	3		
4.	AL18004	Artificial Intelligence and Optimization Techniques	PE	4	3	0	0	3		
5.	AL18005	Design and Analysis of Computer Algorithms	PE	4	3	0	0	3		
6.	AL18006	Hardware and Software Co Design	PE	4	3	0	0	3		
7.	AL18007	Introduction to MEMS System Design	PE	4	3	0	0	3		
8.	AL18008	System on Chip Design	PE	4	3	0	0	3		
9.	AL18009	Selected Topics in ASIC Design	PE	4	3	0	0	3		
10.	AL18010	Selected Topics in IC Design	PE	4	3	0	0	3		
11	AL18011	Signal Integrity For High Speed Design	PE	4	3	0	0	3		
12	AL18012	Wireless Sensor Networks (Common to AL & CU)	PE	4	3	0	0	3		
13	AL18013	Low Power VLSI Design	PE	4	3	0	0	3		
14	AL18014	Solid State Device Modeling And simulation	PE	4	3	0	0	3		
15	AL18015	Testing of VLSI Circuits	PE	4	3	0	0	3		
16	AL18016	VLSI Signal	PE	4	3	0	0	3		

		Processing								
17	AL18017	CAD For VLSI Circuits	PE	4	3	0	0	3		
18	AL18018	DSP Integrated circuits	PE	4	3	0	0	3		
19	AL18019	Advanced Digital Image Processing (Common to AL & CU)	PE	4	3	0	0	3		
20	CU18015	Mobile Adhoc Networks (Common to AL & CU)	PE	3	3	0	0	3		

Summary

Subject Area	**I**	**II**	**III**	**IV**	**Total**
Foundation Course	4	-	-	-	**4**
Professional Subjects-Core (PC), relevant to the chosen specialization/branch; (May be split into Hard (no choice) and Soft (with choice), if required)	13	10	-		**23**
Professional Subjects – Electives (PE), relevant to the chosen specialization/ branch	3	6	9	-	**18**
Mandatory Subjects - (MC)	-	2	-	-	**2**
Project Work, Seminar and/or Internship in Industry or Elsewhere (EEC)	-	2	6	12	**20**
Total Credits	**20**	**20**	**15**	**12**	**67**

MA18181	APPLIED MATHEMATICS FOR ENGINEERS	L	T	P	C
	(Common to PED, Communication systems and Applied Electronics)	**3**	**1**	**0**	**4**

OBJECTIVES:

- To develop the ability to use the concepts of Linear algebra and Special functions for solving problems related to Networks.
- To formulate and construct a mathematical model for a linear programming problem in real life situation;
- To expose the students to solve ordinary differential equations by various techniques.

UNIT I	**LINEAR ALGEBRA**	**12**

Vector spaces – norms – Inner Products – Eigen values using QR transformations – QR factorization - generalized eigenvectors – Canonical forms – singular value decomposition and applications - pseudo inverse – least square approximations --Toeplitz matrices and some applications.

UNIT II	**LINEAR PROGRAMMING**	**12**

Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models

UNIT III	**ORDINARY DIFFERENTIAL EQUATIONS**	**12**

Runge Kutta Methods for system of IVPs, numerical stability, Adams-Bashforth multistep method, solution of stiff ODEs, shooting method, BVP: Finite difference method, orthogonal collocation method, orthogonal collocation with finite element method, Galerkin finite element method.

UNIT IV	**TWO DIMENSIONAL RANDOM VARIABLES**	**12**

Joint distributions – Marginal and Conditional distributions – Functions of two dimensional random variables – Regression Curve – Correlation**.**

UNIT V	**QUEUEING MODELS**	**12**

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.

TOTAL: (L:45 + T:15): 60 PERIODS

OUTCOMES:

- To achieve an understanding of the basic concepts of algebraic equations and method of solving them.
- To familiarize the students with special functions and solve problems associated with Engineering applications.

TEXT BOOKS:

1. Erwin Kreyszig, Advanced Engineering Mathematics, 8th Edition, John Wiley, (1999)
2. Bali N. P and Manish Goyal, "A Text book of Engineering Mathematics", Eighth Edition, Laxmi Publications Pvt Ltd., (2011).
3. Grewal. B.S, "Higher Engineering Mathematics", 41st Edition, Khanna Publications, Delhi, (2011).

REFERENCES:

1. Richard Bronson, Gabriel B.Costa, “Linear Algebra”, Academic Press, Second Edition, 2007.
2. Richard Johnson, Miller & Freund, “Probability and Statistics for Engineers”, 7th Edition,
3. Prentice – Hall of India, Private Ltd., New Delhi (2007).Taha H.A., “Operations Research: An introduction”, Pearson Education Asia, New Delhi, Ninth Edition, 2012.
4. Donald Gross and Carl M. Harris, “Fundamentals of Queueing Theory”, 2nd edition, John Wiley and Sons, New York (1985).
5. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing,Pearson Education, 2000.

AL18101	ADVANCED DIGITAL SIGNAL PROCESSING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To enable the student to understand the basic principles of random signal processing , spectral estimation methods and adaptive filter algorithms and their applications.
- To enable the student to understand the different signal detection and estimation methods used in communication system design and the implications of proper synchronization methods for proper functioning of the system.

UNIT I	**FIR AND IIR FILTERS**	**9**

Overview of DSP, Characterization in time and frequency, FFT Algorithms, Digital filter design and structures: Basic FIR/IIR filter design &structures, design techniques of linear phase FIR filters, IIR filters by impulse invariance, bilinear transformation, FIR/IIR Cascaded lattice structures, and Parallel all pass realization of IIR.

UNIT II	**DSP APPLICATIONS**	**9**

Multi rate DSP, Decimators and Interpolators, Sampling rate conversion, multistage decimator & interpolator, poly phase filters, QMF, digital filter banks, Applications in subband coding. Application of DSP & Multi rate DSP, Application to Radar

UNIT III	**LINEAR ESTIMATION AND PREDICTION**	**9**

Linear prediction & optimum linear filters, stationary random process, forward-backward linear prediction filters, solution of normal equations, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filters for Filtering and Prediction.

UNIT IV	**ADAPTIVE FILTERS**	**9**

Adaptive Filters, Applications, Gradient Adaptive Lattice, Minimum mean square criterion, LMS algorithm, Recursive Least Square algorithm

UNIT V	**SPECTRAL ESTIMATION**	**9**

Estimation of Spectra from Finite-Duration Observations of Signals. Nonparametric Methods for Power Spectrum Estimation,Parametric Methods for Power Spectrum Estimation, Minimum-Variance Spectral Estimation, Eigenanalysis Algorithms for Spectrum Estimation.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

At the end of this course, students will be able to

- To understand theory of different filters and algorithms
- To understand theory of multirate DSP, solve numerical problems and write algorithms
- To understand theory of prediction and solution of normal equations
- To know applications of DSP at block level.

TEXT BOOKS:

1.	J.G.Proakis and D.G.Manolakis"Digital signal processing: Principles, Algorithm and Applications", 4th Edition, Prentice Hall, 2007.
2.	N. J. Fliege, "Multirate Digital Signal Processing: Multirate Systems -Filter Banks –

	Wavelets", 1st Edition, John Wiley and Sons Ltd, 1999.
3.	Bruce W. Suter, "Multirate and Wavelet Signal Processing",1st Edition, Academic Press, 1997.
4	M. H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley & Sons Inc., 2002.
5	S.Haykin, "Adaptive Filter Theory", 4th Edition, Prentice Hall, 2001.
6	D.G.Manolakis, V.K. Ingle and S.M.Kogon, "Statistical and Adaptive Signal Processing", McGraw Hill, 2000.

AL18102	ANALOG INTEGRATED CIRCUIT DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- Analog circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology.
- The basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course.
- The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail

UNIT I	**SINGLE STAGE AMPLIFIERS**	**12**

Basic MOS physics and equivalent circuits and models, CS,, CG and Source Follower cascode and folded cascade configurations, differential amplifiers and current mirror configurations. .

UNIT II	**HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS**	**9**

Current mirrors, cascode stages for current mirrors, current mirror loads for differential pairs. Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascode and differential pair stages Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III	**FEEDBACK AND OPERATIONAL AMPLIFIERS**	**9**

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV	**STABILITY AND FREQUENCY COMPENSATION**	**9**

General considerations, Multipole systems,Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.

UNIT V	**BANDGAP REFERENCES**	**6**

Supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

TOTAL: (L: + T:): 45 PERI ODS

OUTCOMES:

- Determine the device dimensions of MOSFETs.
- Discuss the most important building blocks of all CMOS analog ICs.
- Analyze the basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design.
- Design single and multistage voltage, current and differential amplifiers..

REFERENCES:

1.	Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill, 2001
2.	Willey M.C. Sansen, “Analog Design Essentials”, Springer, 2006
3.	Grebene, “Bipolar and MOS Analog Integrated circuit design”, John Wiley & sons,Inc., 2003.
4.	Phillip E.Allen, DouglasR.Holberg, “CMOS Analog Circuit Design”, Second edition, Oxford University Press, 2002
5.	Recorded lecture available at http://www.ee.iitm.ac.in/~ani/ee5390/index.html Jacob Baker “CMOS: Circuit Design, Layout, and Simulation, Third Edition”, Wiley IEEE Press 2010 3rd Edition

AL18103	EMBEDDED SYSTEMS DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To expose the students to the fundamentals of embedded system design.
- To enable the students to understand and use embedded computing platform.
- To introduce networking principles in embedded devices.
- To introduce RTOS in embedded devices.

UNIT I	**EMBEDDED PROCESSORS**	**12**

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.

UNIT II	**EMBEDDED PROCESSOR AND COMPUTING PLATFORM**	**9**

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture

UNIT III	**NETWORKS**	**9**

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV	**REAL-TIME CHARACTERISTICS**	**9**

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

UNIT V	**SYSTEM DESIGN TECHNIQUES**	**6**

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer-Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- Able to select and design suitable embedded systems for real world applications.

TEXT BOOKS:

1. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers.

2.	Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia
3	C. M. Krishna and K. G. Shin, “Real-Time Systems” , McGraw-Hill, 1997
4	Frank Vahid and Tony Givargis, “Embedded System Design: A Unified Hardware/Software Introduction” , John Wiley & Sons.

AL18111	EMBEDDED SYSTEMS DESIGN LABORATORY	L	T	P	C
		0	0	4	2

OBJECTIVES:

- To give a hands on programming experience using microcontrollers.
- To induce a programming skill in embedded system design using KEIL or RIDE software.

LIST OF EXPERIMENTS:

1.Board development using microcontroller
2.Assembly and High level language programs for microcontroller - ports – timers - Seven Segment display – I^2C – LCD interface
3.RTOS – Simple task creation, Round Robin Scheduling, Preemptive scheduling, Semaphores, Mailboxes.
4.Assembly and High level language programs for R8C - ports – timers -Seven Segment display – I^2C – LCD interface – Stepper Motor control
5.Assembly and High level language programs for MSP 430 - ports – timers - Seven Segment display – I^2C – LCD interface – Stepper Motor control

TOTAL: 60 PERIODS

OUTCOMES:

- Ability to gain the skill of effective design of embedded systems using different microcontrollers.

List of Equipment for Batch of 18 students:

Sl No	Description of equipment	Quantity required
1.	ARM 7 Trainer Kit with Software	4
2.	PC'S	4
3.	MSP430 Microcontroller	4
4.	Seven Segment display	3
5.	LCD interface	3
6.	Stepper Motor	3

CU18112	ADVANCED DIGITAL SIGNAL PROCESSING LABORATORY	L	T	P	C
		0	0	4	2

Course Objective:

- To introduce simulation tools and software to represent a signal in various forms
- To familiarize in using various digital filters
- To perform the power spectrum analysis

LIST OF EXPERIMENTS:

1.	Basic Signal Representation
2.	Correlation Auto And Cross
3.	Stability Using Hurwitz Routh Criteria
4.	Sampling FFT Of Input Sequence
5.	Butterworth Lowpass And Highpass Filter Design
6.	Chebychev Type I,II Filter
7.	State Space Matrix from Differential Equation
8.	Normal Equation Using Levinson Durbin
9.	Decimation And Interpolation Using Rationale Factors
10.	Maximally Decimated Analysis DFT Filter
11.	Cascade Digital IIR Filter Realization
12.	Convolution And M Fold Decimation &PSD Estimator
13	Estimation Of PSD
14.	Inverse Z Transform

Course Outcomes: At the end of this course, students will be able to

- Design different digital filters in software
- Apply various transforms in time and frequency
- Perform decimation and interpolation

TOTAL:60 PERIODS

List of Equipment for Batch of 18 students:

Sl No	Description of equipment	Quantity required
1.	PCs	10
2.	MATLAB with Simulink and Signal Processing Tool Box or Equivalent Software in desktop systems	5

II SEMESTER

AL18201	ASIC AND FPGA DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To study the design flow of different types of ASIC.
- To familiarize the different types of programming technologies and logic devices.
- To learn the architecture of different types of FPGA.
- To gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC

UNIT I	**OVERVIEW OF ASIC AND PLD**	**9**

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

UNIT II	**ASIC PHYSICAL DESIGN**	**9**

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction – DRC

UNIT III	**LOGIC SYNTHESIS, SIMULATION AND TESTING**	**9**

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT IV	**FIELD PROGRAMMABLE GATE ARRAYS**	**9**

FPGA Design : FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

UNIT V	**SOC DESIGN**	**9**

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies: Canonical Signed Digit Arithmetic, Knowledge Crunching Machine, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- To analyze the synthesis, Simulation and testing of systems.
- To apply different high performance algorithms in ASICs.
- To discuss the design issues of SOC.

REFERENCES:

1. David A.Hodges, Analysis and Design of Digital Integrated Circuits (3/e), MGH 2004

2.	H.Gerez, Algorithms for VLSI Design Automation, John Wiley, 1999
3.	Jan. M. Rabaey et al, Digital Integrated Circuit Design Perspective (2/e), PHI 2003
4.	M.J.S. Smith : Application Specific Integrated Circuits, Pearson, 2003
5.	J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.
6	P.K.Chan& S. Mourad, Digital Design using Field Programmable Gate Array, Prentice Hall.
7	Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier, 2008
8	S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Pub.
9	S.Brown,R.Francis, J.Rose, Z.Vransic, Field Programmable GateArray, Kluwer Pub

AL18202	ANALOG AND DIGITAL CMOS VLSI DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn the physical design flow of CMOS design
- To familiarize with the sequential logic design using CMOS
- To implement various amplifier types and mirror circuits using CMOS

UNIT I **9**

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design:Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

UNIT II **9**

Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic,Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates,CMOS transmission gate logic

UNIT III **9**

Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers,Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

UNIT IV **9**

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT V **9**

Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES: At the end of this course, students will be able to

- Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.
- Connect the individual gates to form the building blocks of a system.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice.

REFERENCES:	
1.	J P Rabaey, A P Chandrakasan, B Nikolic, “Digital Integrated circuits: A design perspective”, Prentice Hall electronics and VLSI series, 2nd Edition.
2.	Baker, Li, Boyce, “CMOS Circuit Design, Layout, and Simulation”, Wiley, 2nd Edition.
3.	BehzadRazavi , “Design of Analog CMOS Integrated Circuits”, TMH, 2007.
4.	Phillip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford, 3rd Edition.
5.	R J Baker, “CMOS circuit Design, Layout and Simulation”, IEEE Inc., 2008.
6	Kang, S. and Leblebici, Y., “CMOS Digital Integrated Circuits, Analysis and Design”,
7	Pucknell, D.A. and Eshraghian, K., “Basic VLSI Design”, PHI, 3rd Edition.

MC18081	INTRODUCTION TO RESEARCH METHODOLOGY AND IPR	L	T	P	C
		2	0	0	2

OBJECTIVES:

- To impart knowledge on formulation of research problem, research methodology, ethics involved in doing research and importance of IPR protection.

UNIT I	**RESEARCH METHODOLOGY**	**6**

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, Plagiarism, Research ethics

UNIT II	**RESULTS AND ANALYSIS**	**6**

Importance and scientific methodology in recording results, importance of negative results, different ways of recording, industrial requirement, artifacts versus true results, types of analysis (analytical, objective, subjective), outcome as new idea, hypothesis, concept, theory, model etc.

UNIT III	**TECHNICAL WRITING**	**6**

Effective technical writing, how to write a manuscript/ responses to reviewers comments, preparation of research article/ research report, Writing a Research Proposal - presentation and assessment by a review committee

UNIT IV	**INTELLECTUAL PROPERTY RIGHTS**	**6**

Nature of Intellectual Property: Patents, Designs, Trade Mark and Copyright. Process of Patenting and Development: technological research, innovation, patenting & development. Procedure for grants of patents, Patenting under PCT.

UNIT V	**PATENT RIGTS AND NEW DEVELOPMENTS IN IPR**	**6**

Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System.

TOTAL: (L: + T:): 30 PERIODS

OUTCOMES:

At the end of this course, students will be able to

- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understand research problem formulation & Analyze research related information and Follow research ethics
- Correlate the results of any research article with other published results. Write a review article in the field of engineering.

• Appreciate the importance of IPR and protect their intellectual property. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits	
TEXT BOOKS:	
1.	Ranjit Kumar, Research Methodology- A step by step guide for beginners, Pearson Education, Australia, 2005.
2.	Ann M. Korner, Guide to Publishing a Scientific paper, Bioscript Press 2004.
3.	T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008
REFERENCES:	
1.	Kothari, C. R. Research Methodology - Methods and Techniques, New Age International publishers, New Delhi, 2004.
2.	Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students', Juta & Company, 1996.
3.	Robert P. Merges, Peter S. Menell and Mark A. Lemley, "Intellectual Property in New Technological Age", Aspen Publishers, 2016.
4	Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
5	Mayall , "Industrial Design", McGraw Hill, 1992.
6	Niebel , "Product Design", McGraw Hill, 1974.
7	Asimov , "Introduction to Design", Prentice Hall, 1962.

AL18211	INTEGRATED CIRCUIT DESIGN LABORATORY	L	T	P	C
		0	0	4	2

OBJECTIVES:

- To introduce the programming concepts using Verilog or VHDL
- To introduce the concepts of system design using FPGA

LIST OF EXPERIMENTS:

1. Design Entry Using VHDL or Verilog, examples for circuit descriptions using HDL languages sequential and concurrent statements.
2.Structural and behavioral descriptions, principles of operation and limitation of HDL simulators. Examples of sequential and combinational logic design and simulation. Test vector generation.
3.CPLD – Board development. I/O interfacing, Analog interfacing, Real time application development.
4.FPGA- Board development. I/O interfacing, Analog interfacing, Real time application development.
5.System development using either PSPICE or FPGA.

TOTAL: 60 PERIODS

OUTCOMES:

- Ability to develop FPGA based system design.

List of Equipment for Batch of 18 students:

Sl No	Description of equipment	Quantity Required
1.	EDA tools :Cadence /Tanner / Mentor Graphics / open source software tools like Ngspice.	4 User License
2.	Xilinx tool	4 No’s
3.	PCs	4 No’s
4.	CPLD	3 No’s
5.	FPGA Board (SPARTAN-6 & SPARTAN-6E)	4 No’s

AL18212	ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY	L	T	P	C
		0	0	4	2

OBJECTIVES:

- To introduce the programming concepts using Verilog or VHDL
- To introduce the concepts of system design using FPGA

LIST OF EXPERIMENTS:

1. Use VDD=1.8V for 250 nm CMOS process, VDD=1.3V for 250 nm CMOS Process and VDD=1V for 0.09um CMOS Process.

a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.

b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.

c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.

d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.

e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30mV To extract Vth use the following procedure.

i. Plot gm vs VGS using SPICE and obtain peak gm point.

ii. Plot y=ID/(gm)1/2 as a function of VGS using SPICE.

iii. Use SPICE to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.

f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate your result according to technologies and comment on it.

2. Use VDD=1.8V for 250 nm CMOS process, VDD=1.2V for 250 nm CMOS Process and VDD=1V for 0.09um CMOS Process.

a) Perform the following

i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.

ii. Plot VTC for CMOS inverter with varying VDD.

iii. Plot VTC for CMOS inverter with varying device ratio.

b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF)

c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Cload = 4pF, Rload = k).

3. Use SPICE to build a three stage and five stage ring oscillator circuit in 250 nm and 250 nm technology and compare its frequencies and time period.

Perform the following

a) Draw small signal voltage gain of the minimum-size inverter in 250 nm and 250 nm technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using SPICE and compare the values for 250 nm and 250 nm process.

b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 250 nm technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.

i. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2.

ii. Calculate input bias voltage if bias current=50uA.

iii. Use SPICE and obtain the bias current. Compare its value with 50uA.

iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in SPICE (consider 30fF load capacitance).

v. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time

constant of the output and compare it with the time constant resulted from -3dB BW

vi. Use SPICE to determine input voltage range of the amplifier.

Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA. Note:

4. Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

i. Draw the schematic of op-amp macro model.

ii. Draw the schematic of INA.

iii. Obtain parameters of the op-amp macro model such that

a. low-frequency voltage gain = 5x104,

b. unity gain BW (fu) = 500KHz,

c. input capacitance=0.2pF,

d. output resistance =_,

e. CMRR=120dB

iv. Draw schematic diagram of CMRR simulation setup.

v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.

Technology: UMC 250 nm, VDD=1.8V. Use SPICE.

5. a) Draw layout of a minimum size inverter in UMC 250 nm technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.

b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.

c) Use extracted netlist and obtain tPHLtPLH for the middle inverter using SPICE.

d) Use interconnect length obtained and connect the second and third inverter.

Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part ‘c’.

	TOTAL: 60 PERIODS	

OUTCOMES:

At the end of the laboratory work, students will be able to:

- Design digital and analog Circuit using CMOS.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice.

List of Equipment for Batch of 18 students:

Sl No	Description of equipment	Quantity required
1.	EDA tools :Cadence/Tanner/Mentor Graphics / open source software tools like Ngspice.	4 User License
2.	PC’s	4 No’s

AL18213	MINI PROJECT	L	T	P	C
		0	0	4	2

Course Outcome

- The student will solve a live problem using software/analytical/computational tools.
- Students will learn to write technical reports.
- Students will develop skills to present and defend their work in front of technically qualified audience.
- To introduce the configuration process of networking devices.
- To work with the client and server.

SYLLABUS CONTENT:

Students can take up small problems in the field of communication engineering as mini project. It can be related to solution to an engineering problem, verification and analysis of experimental data available, conducting experiments on various engineering subjects, characterization, studying a software tool for the solution of an engineering problem etc.

	TOTAL:60 PERIODS

ELECTIVES

AL18001	INTERNET OF THINGS FOR ELECTRONICS ENGINEERS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introduce the concept of Internet of Things and its associated terms
- To familiarize with sensor networks and its association with IoT
- To inculcate the various operating systems used in IoT and its reach towards aiding mankind.

UNIT I	**12**

Smart cities and IoT revolution, Fractal cities, From IT to IoT, M2M and peer networking concepts, Ipv4 and IPV6. Software Defined Networks SDN, From Cloud to Fog and MIST networking for IoT communications, Principles of Edge/P2P networking, Protocols to support IoT communications, modular design and abstraction, security and privacy in fog.

UNIT II	**8**

Wireless sensor networks: introduction, IOT networks (PAN, LAN and WAN), Edge resource pooling and caching, client side control and configuration.

UNIT III	**8**

Smart objects as building blocks for IoT, Open source hardware and Embedded systems platforms for IoT, Edge/gateway, IO drivers, C Programming, multithreading concepts.

UNIT IV	**8**

Operating systems requirement of IoT environment, study of mbed, RIoT, and Contiki operating systems, Introductory concepts of big data for IoT applications.

UNIT V	**9**

Applications of IoT, Connected cars IoT Transportation, Smart Grid and Healthcare sectors using IoT, Security and legal considerations, IT Act 2000 and scope for IoT legislation.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- Able to know the various networking concepts related to IoT
- Able to design an IoT module using various operating systems and programming skills

REFERENCES:

1.	A Bahaga, V. Madisetti, “Internet of Things- Hands on approach”, VPT publisher, 2014.
2.	A. McEwen, H. Cassimally, “Designing the Internet of Things”, Wiley, 2013.
3.	CunoPfister, “Getting started with Internet of Things”, Maker Media, 1st edition, 2011.
4.	Samuel Greenguard, “Internet of things”, MIT Press, 2015.

Web resources :

http://www.datamation.com/open-source/35-open-source-tools-for-the-internet-of-things-
https://developer.mbed.org/handbook/AnalogIn
http://www.libelium.com/50_sensor_applications/M2MLabs Mainspring

	http://www.m2mlabs.com/frameworkNode-RED http://nodered.org/

AL18002	SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- Deals with the basics of synthesis optimization, scheduling algorithms and resource allocation algorithms for CAD synthesis.
- To teach the logic level synthesis for combinational as well as sequential circuits and technology mapping.

UNIT I	**CIRCUITS AND HARDWARE MODELING**	**9**

Design of Microelectronic Circuits - Computer Aided Synthesis and optimization-Combinatorial optimization-Boolean Algebra and Application-Hardware Modeling Languages –Compilation and Behavioral optimization.

		9
UNIT II	**ARCHITECTURAL LEVEL SYNTHESIS AND OPTIMIZATION**	

The Fundamental Architectural synthesis Problems-Area and performance Estimation-Control unit synthesis-synthesis of pipelined circuits.

UNIT III	**SCHEDULING ALGORITHMS AND RESOURCE SHARING**	**9**

Unconstrained Scheduling-ASAP Algorithm-ALAP Scheduling Algorithm- Scheduling with Resource Constraints- Scheduling pipelined circuits-Sharing and binding for Dominated circuits-Area Binding-Concurrent Binding –Module selection problems-Structural testability.

UNIT IV	**LOGIC-LEVEL SYNTHESIS AND OPTIMIZATION**	**9**

Logic optimization Principles-Algorithms and logic Minimization –Encoding problems- Multiple-level optimization of logic networks-Algebraic and Boolean model-Algorithm for delay Evaluation-Rule based logic optimization.

UNIT V	**SEQUENTIAL LOGIC OPTIMIZATION**	**9**

Sequential circuit -State Encoding-Minimization methods-Retiming- Finite state machine-testability for synchronous circuits-Algorithm for library binding- Look-Up table - FPGA- Rule-based library binding

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- Capability to design , synthesize and optimize combinational as well as sequential circuits.
- Ability to modify the digital designs for optimal performance using different scheduling and resource allocation algorithms

REFERENCES:

1. Giovanni De Micheli, “Synthesis and optimization of Digital Circuits”, Tata McGraw-Hill, 2003.
2. John Paul Shen, Mikko H. Lipasti, “Modern processor Design”, Tata McGraw Hill, 2003

AL18003	ADVANCED MICROPROCESSORS AND MICROCONTROLLERS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To expose the students to the fundamentals of microprocessor architecture.
- To introduce the advanced features in microprocessors and microcontrollers.
- To enable the students to understand various microcontroller architectures.

UNIT I	**MICROPROCESSOR ARCHITECTURE**	**9**

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards– instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

UNIT II	**HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM**	**9**

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

UNIT III	**HIGH PERFORMANCE RISC ARCHITECTURE – ARM**	**9**

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor

UNIT IV	**MOTOROLA 68HC11 MICROCONTROLLERS**	**9**

Instruction set addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART.

UNIT V	**PIC MICROCONTROLLER**	**9**

CPU Architecture – Instruction set – interrupts- Timers- I^2C Interfacing –UART- A/D Converter – PWM and introduction to C-Compilers

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- The student will be able to work with suitable microprocessor / microcontroller for a specific real world application.

REFERENCES:

1.	Daniel Tabak , „‟ Advanced Microprocessors” McGraw Hill.Inc., 1995
2.	James L. Antonakos , “ The Pentium Microprocessor „‟ Pearson Education , 1997
3.	Steve Furber , „‟ ARM System –On –Chip architecture “Addision Wesley , 2000
4.	Gene .H.Miller .” Micro Computer Engineering ,” Pearson Education , 2003
5.	John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.
6.	James L.Antonakos ,” An Introduction to the Intel family of Microprocessors „‟ Pearson

	Education 1999.
7.	Barry.B.Breg," The Intel Microprocessors Architecture , Programming and interfacing " , PHI,2002.
8.	Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001. Readings: Web links www.ocw.nit.edu www.arm.com

AL18004	ARTIFICIAL INTELLIGENCE AND OPTIMIZATION TECHNIQUES	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introduce the techniques of computational methods inspired by nature, such as neural networks, genetic algorithms and other evolutionary computation systems, ant swarm optimization, artificial immune systems, cellular automata, and multi-agent systems.
- To present main rules underlying in these techniques.
- To present selected case-studies.
- To adopt these techniques in solving problems in the real world.

UNIT I	**NEURAL NETWORKS**	**9**

Neural Networks: Back Propagation Network, generalized delta rule, Radial Basis Function Network, interpolation and approximation RBFNS, comparison between RBFN and BPN, Support Vector Machines : Optimal hyperplane for linearly separable patterns, optimal hyperplane for non-linearly separable patterns, Inverse Modeling.

UNIT II	**FUZZY LOGIC SYSTEMS**	**9**

Fuzzy Logic System: Basic of fuzzy logic theory , crisp and fuzzy sets, Basic set operation like union , interaction , complement , T-norm , T-conorm , composition of fuzzy relations, fuzzy if-then rules , fuzzy reasoning, Neuro-Fuzzy Modeling: Adaptive Neuro-Fuzzy Inference System (ANFIS) , ANFIS architecture , Hybrid Learning Algorithm.

UNIT III	**EVOLUTIONARY COMPUTATION AND GENETIC ALGORITHMS**	**9**

Evolutionary Computation (EC) – Features of EC – Classification of EC – Advantages – Applications. Genetic Algorithms: Introduction – Biological Background – Operators in GA-GA Algorithm – Classification of GA – Applications

UNIT IV	**ANT COLONY OPTIMIZATION**	**9**

Ant Colony Optimization: Introduction – From real to artificial ants- Theoretical considerations – Convergence proofs – ACO Algorithm – ACO and model based search – Application principles of ACO.

UNIT V	**PARTICLE SWARM OPTIMIZATION**	**9**

Particle Swarm Optimization: Introduction – Principles of bird flocking and fish schooling – Evolution of PSO – Operating principles – PSO Algorithm – Neighborhood Topologies – Convergence criteria – Applications of PSO, Honey Bee Social Foraging Algorithms, Bacterial Foraging Optimization Algorithm.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

Upon completion of the course, students will be able to:

- Design of the fundamental Computational Intelligence models
- Apply the concepts of neural networks, genetic algorithms, fuzzy neural networks, and ant

colony optimization algorithms

- Application of computational Intelligence techniques to classification, pattern recognition, prediction, rule extraction, and optimization problems.

REFERENCES:

1.	Christopher M. Bishop, “Neural Networks for Pattern Recognition”, Oxford University Press
2.	Nello Cristianini, John Shawe-Taylor, "An Introduction to Support Vector Machines and Other Kernel-based Learning Methods”,Cambridge University Press.
3.	Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani,” Neuro-fuzzy and soft computing: a computational approach to learning and machine intelligence”, Prentice Hall of India, New Delhi. H.-J. Zimmermann, “Fuzzy Set Theory and its Applications”, Springer.
4.	David E. Goldberg, “Genetic Algorithms in search, Optimization & Machine Learning”, Pearson Education.
5.	Kenneth A DeJong,“Evolutionary Computation A Unified Approach”, Prentice Hall of India, New Delhi.
6	Marco Dorigo and Thomas Stutzle, “Ant Colony optimization”, Prentice Hall of India, New Delhi.
7.	N P Padhy, Artificial Intelligence and Intelligent Systems, Oxford University Press, 2005
8.	Engelbrecht, A.P. Fundamentals of Computational Swarm Intelligence, Wiley.

AL18005	DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- Discusses the algorithmic complexity parameters and the basic algorithmic design techniques.
- To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms and NP Hard Problems

UNIT I	**INTRODUCTION**	**9**

Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II	**DESIGN TECHNIQUES**	**9**

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III	**SEARCHING AND SORTING**	**9**

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

UNIT IV	**GRAPH ALGORITHMS**	**9**

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms,max-flow min cut theorem, Steiglitz's link deficit algorithm.

UNIT V	**GRAPH ALGORITHMS**	**9**

NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- Will be able to apply the suitable algorithm according to the given optimization problem.
- Ability to modify the algorithms to refine the complexity parameters.

REFERENCES:

1.	Ara Baase, "Computer Algorithms : Introduction to Design and Analysis", Addison Wesley, 1988.
2.	T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill, 1994
3.	E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia Publications, 1988
4.	D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison Wesley, 1989

AL18006	HARDWARE AND SOFTWARE CO DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- The students will learn various design steps starting fromsystem specifications to willhardware/software implementation andexperience process optimization whileconsidering various design steps.
- Students will gain design experience with project/case studies using contemporary high-level methods and tools.

UNIT I	SYSTEM SPECIFICATION AND MODELLING	9

Embedded Systems , Hardware/Software Co-Design , Co-Design for System Specification and Modelling Co-Design for Heterogeneous Implementation - Processor Synthesis , Single-Processor Architectures with one ASIC , Single-Processor Architectures with many ASICs, Multi-Processor Architectures , Comparison of Co-Design Approaches , Models of Computation ,Requirements for Embedded System Specification .

UNIT II	HARDWARE/SOFTWARE PARTITIONING	9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph , Formulation of the HW/SW Partitioning Problem , Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms .

UNIT III	HARDWARE/SOFTWARE CO-SYNTHESIS	9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation,Distributed System Co-Synthesis

UNIT IV	PROTOTYPING AND EMULATION	9

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping ,Target Architecture- Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems

UNIT V	DESIGN SPECIFICATION AND VERIFICATION	9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification , Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

On completion of the course, a student should be able:

- To outline and apply design methodologies
- To appreciate the fundamental building blocks of the using hardware and software co-design and related implementation and testing environments and techniques and their inter-relationships

• To modern hardware/software tools for building prototypes • To demonstrate practical competence in these areas.		
REFERENCES:		
1.	Ralf Niemann , “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998	
2.	Jorgen Staunstrup , Wayne Wolf ,”Hardware/Software Co-Design: Principles and Practice”Kluwer Academic Pub,1997	
3.	Giovanni De Micheli , Rolf Ernst Morgon,” Reading in Hardware/Software Co-Design Kaufmann Publishers,2001	

AL18007	INTRODUCTION TO MEMS SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To give hands on experience for the fabrication processes using micro-fabrication tools in the cleanroom.
- Briefly review on various application fields of the microsensors, MEMS, and smart devices. The materials and the processes required to make different kinds of the microdevices.
- The standard microelectronics technology to produce ultra large-scale integrated circuits and package them will also be reviewed. The new techniques that have been developed to make microsensors and microactuators, such as bulk and surface silicon micromachining will be followed.

UNIT I	**INTRODUCTION TO MEMS**	**9**

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Microaccelorometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II	**MECHANICS FOR MEMS DESIGN**	**9**

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III	**ELECTRO STATIC DESIGN**	**9**

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV	**CIRCUIT AND SYSTEM ISSUES**	**9**

Electronic Interfaces, Feed back systems, Noise , Circuit and system issues, Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS

UNIT V	**INTRODUCTION TO OPTICAL AND RF MEMS**	**9**

Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

On completion of the module students should:

- Be able to extend the principles of microfabrication to the development of micromechanical devices and the design of microsystems
- Understand the principles of energy transduction, sensing and actuation on a microscopic scale.

• Appreciate the effects of scaling, and the similarities and differences between micromechanical assemblies and macroscopic machines	
TEXT BOOKS:	
1.	Stephen Santuria," Microsystems Design", Kluwer publishers, 2000.
REFERENCES:	
1.	Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House, 2000
2.	Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton,2000.
3.	Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002

AL18008	SYSTEM ON CHIP DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- Understanding of the concepts, issues, and process of designing highly integrated SoCs following systematic hardware/software co-design & co-verification principles

UNIT I	**INTRODUCTION**	**9**

Introduction to SoC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, real time scheduling, embedded OS, middle ware; Platform based SoC design, multiprocessor SoC and Network on Chip, Low power SoC Design

UNIT II	**SYSTEM LEVEL MODELLING**	**9**

SystemC: overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples

UNIT III	**HARDWARE SOFTWARE CO-DESIGN**	**9**

Analysis, partitioning, high level optimisations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems.

UNIT IV	**SYNTHESIS**	**9**

System synthesis: Transaction Level Modelling (TLM) based design, automaticTLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimisation, resource sharing and pipelining and scheduling

UNIT V	**SOC VERIFICATION AND TESTING**	**9**

SoC and IP integration, Verification : Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modeling, test power dissipation, test access mechanism

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- Analyse algorithms and architecture of hardware software inorder to optimise the system based on requirements and implementation constraints
- Model and specify systems at high level of abstractionappreciate the co-design approach and virtual platform models
- Understand hardware, software and interface synthesis

REFERENCES:

1.	D. Black, J. Donovan, SystemC: From the Ground Up, Springer, 2004.
2.	D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Embedded System Design: Modeling,

	Synthesis, Verification, Springer, 2009
3	Erik Larson, Introduction to advanced system-on-chip test design and optimisation, Springer 2005
4	Grotker, T., Liao, S., Martin, G. & Swan, S. System design with System C, Springer, 2002.
5	Ghenassia, F. Transaction-level modeling with SystemC: TLM concepts and applications for embedded systems, Springer, 2010.
6	Hoi-junyoo, Kangmin Lee, Jun Kyoungkim, "Low power NoC for high performance SoCdesing",CRC press, 2008.
7	M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2005
8	M. Abramovici, M. Breuer, and A. Friedman, Digital System Testing and Testable Design, IEEE Press, 1994
9	P. Marwedel, Embedded System Design, Springer, 2003. G. De Micheli, Synthesis and Optimization of Digital Circuits
10	Prakash Rashinkar, Peter Paterson and Leena Singh, System-on-a chip verification: Methodology and techniques, kluwer Academic Publishers 2002
11	T. Noergaard, Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers, Newnes.
12	Vijay K. MadisettiChonlamethArpikanondt, "A Platform-Centric Approach to System-onChip (SOC) Design", Springer, 2005. 13. Youn-Long St

AL18009	SELECTED TOPICS IN ASIC DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- The course focuses on the semi custom IC Design and introduces the principles of design logic cells, I/O cells and interconnect architecture, with equal importance given to FPGA and ASIC styles.
- The entire FPGA and ASIC design flow is dealt with from the circuit and layout design point of view.

UNIT I	**INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN**	**9**

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II	**PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS**	**9**

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III	**PROGRAMMABLE ASIC ARCHITECUTRE**	**9**

Architecture and configuration of Spartan / Cyclone and Virtex / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT IV	**LOGIC SYNTHESIS, PLACEMENT AND ROUTING**	**9**

Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.

UNIT V	**HIGH PERFORMANCE ALGORITHMS FOR ASICS/ SOCS. SOC CASE STUDIES**	**9**

DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. Case Studies: Digital camera, SDRAM, High speed data standards.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

After completing this course:

- The student would have gained knowledge in the circuit design aspects at the next transistor and block level abstractions of FPGA and ASIC design. In combination with the course on CAD for VLSI, the student would have gained sufficient theoretical knowledge for carrying out FPGA and ASIC designs.

REFERENCES:

1.	M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2003
2.	Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science.
3.	Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation of Signal Processing Systems”, Wiley, 2008

4	Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5	Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996.
6	Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994

AL18010	SELECTED TOPICS IN IC DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introduce supply circuit modules which are crucial modules in an IC design. Clock generation circuits play a major role in High Speed Broad Band Communication circuits, High Speed I/O‟s, Memory modules and Data Conversion Circuits.
- This course focuses on the design aspect of Clock Generation circuits and their design constraints.

UNIT I	**VOLTAGE AND CURRENT REFERENCES**	**9**

Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature independent Biasing, PTAT Current Generation, Constant Gm Biasing

UNIT II	**LOW DROP OUT REGULATORS**	**9**

Analog Building Blocks, Negative Feedback, AC Design, Noise and Noise Reduction Techniques, Stability, LDO Efficiency, LDO Current Source, LDO Current Source Using Opamp.

UNIT III	**OSCILLATOR FUNDAMENTALS**	**9**

General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator,Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for Ring Oscillators, Phase Noise in Differential LC Oscillators

UNIT IV	**PHASE LOCK LOOPS**	**9**

PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLL Building blocks, Jitter and Phase Noise performance.

UNIT V	**CLOCK AND DATA RECOVERY**	**9**

CDR Architectures, Tias and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

TOTAL: (L: + T:):45 PERIODS

OUTCOMES:

- Students will be able construct Supply reference circuits and Clock Generation Circuits for given design specifications and aids to understand the design specifications related to Supply and Clock Generation Circuits

REFERENCES:

1. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgap circuits",John wiley & Sons, Inc 2002.
2. Floyd M. Gardner ,"Phase LocK Techniques" John wiley & Sons, Inc 2005.
3. High Speed Clock and Data Recovery, High-performance Amplifiers Power Management " springer, 2008.
4. Behzad Razavi, " Design of Integrated circuits for Optical Communications", McGraw Hill, 2003.

AL18011	SIGNAL INTEGRITY FOR HIGH SPEED DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

UNIT I	**SIGNAL PROPAGATION ON TRANSMISSION LINES**	**9**

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion

UNIT II	**MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK**	**9**

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-endbcross-talk, minimizing cross-talk (stripline and microstrip) balanced circuits ,S-parameters, Lossy and Lossles models Differential signalling, termination,

UNIT III	**NON-IDEAL EFFECTS**	**9**

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic,Common-mode current, differential-mode current , Connectors

UNIT IV	**POWER CONSIDERATIONS AND SYSTEM DESIGN**	**9**

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis

UNIT V	**CLOCK DISTRIBUTION AND CLOCK OSCILLATORS**	**9**

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL: (L: + T:):45 PERIODS

OUTCOMES:

- Ability to identify sources affecting the speed of digital circuits.
- Able to improve the signal transmission characteristics.

REFERENCES:

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR , 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.

AL18012	WIRELESS SENSOR NETWORKS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To enable the student to understand the role of sensors and the networking of sensed data for different applications.
- To expose the students to the sensor node essentials and the architectural details, the medium access and routing issues and the energy constrained operational scenario.
- To enable the student to understand the challenges in synchronization and localization of sensor nodes, topology management for effective and sustained communication, data management and security aspects.

UNIT I	**OVERVIEW OF WIRELESS SENSOR NETWORKS**	**9**

Challenges for Wireless Sensor Networks-Characteristics requirements-required mechanisms, Difference between mobile ad-hoc and sensor networks, Applications of sensor networks- case study, Enabling Technologies for Wireless Sensor Networks.

UNIT II	**ARCHITECTURES**	**9**

Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes , Operating Systems and Execution Environments, Network Architecture - Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concepts. Physical Layer and Transceiver Design Considerations

		9
UNIT III	**MAC AND ROUTING**	

And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Address and Name Management, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing.

UNIT IV	**INFRASTRUCTURE ESTABLISHMENT**	**9**

Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

UNIT V	**DATA MANAGEMENT and SECIRUTY**	**9**

MAC Protocols for Wireless Sensor Networks, IEEE 802.15.4, Zigbee, Low Duty Cycle Protocols Data management in WSN, Storage and indexing in sensor networks, Query processing in sensor, Data aggregation, Directed diffusion, Tiny aggregation, greedy aggregation, security in WSN.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- The student would be able to appreciate the need for designing energy efficient sensor nodes and protocols for prolonging network lifetime.
- The student would be able to demonstrate an understanding of the different implementation challenges and the solution approaches.

REFERENCES:

1. Ian F. Akyildiz, Mehmet Can Vuran, " Wireless Sensor Networks" John Wiley, 2010
2. Yingshu Li, My T. Thai,Weili Wu, " Wireless Sensor Networks and Applications" Springer 2008
3. Holger Karl & Andreas Willig, " Protocols And Architectures for Wireless Sensor Networks" , John Wiley, 2005.
4. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
5. Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks-s Technology, Protocols, And Applications", John Wiley, 2007.
6. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.
7. Bhaskar Krishnamachari, "Networking Wireless Sensors", Cambridge Press,2005.

AL18013	LOW POWER VLSI DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- Identify the power reduction techniques based on technology Independent and technology dependent
- Power dissipation mechanism in various MOS logic style and identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation.

UNIT I	**POWER DISSIPATION IN CMOS**	**9**

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II	**POWER OPTIMIZATION**	**9**

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers

UNIT III	**DESIGN OF LOW POWER CMOS CIRCUITS**	**9**

Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques.

UNIT IV	**POWER ESTIMATION**	**9**

Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V	**SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER**	**9**

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- The student will apply the basics and advanced techniques in low power design which is a hot topic in today‟s market where the power plays major role.
- The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

REFERENCES:

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002
3. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995.
5. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001.

AL18014	SOLID STATE DEVICE MODELING AND SIMULATION	L	T	P	C
		3	0	0	3

OBJECTIVES:

- The three areas of circuit design, device modeling and CAD tools are the main pillars based on which all VLSI system designs are carried out.
- This course introduces the principles of device modeling wherein device physics and experimentally observed device performance characteristics combined so as to lead to predictable equations and expressions for device performance under various scenarios of excitation.
- The most widely used device models used by the industry including BSIM and EKV models discussed.

UNIT I	**MOSFET DEVICE PHYSICS**	**9**

Band theory of solids, carrier transport mechanism, MOS capacitor - surface potential, accumulation, depletion, inversion, electrostatic potential and charge distribution, threshold voltage, polysilicon work function, interface states and oxide traps, drain current model, sub-threshold characteristics.

UNIT II	**MOSFET MODELING**	**9**

Basic modeling, SPICE Level-1, 2 and 3 models, Short channel effects, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling.

UNIT III	**NOISE MODELING**	**9**

Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuit

UNIT IV	**BSIM4 MOSFET MODELING**	**9**

Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, Mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, Noise model, Junction diode models , Layout-dependent parasitics model

UNIT V	**VOTHER MOSFET MODELS**	**9**

The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, Noise model, temperature effects, MOS model 9, MOSAI model, PSP model, Influence of process variation, Modeling of device mismatch for Analog/RF Applications.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- The student who completes this course will be in a position understand the procedures used to construct the complicated device models that are widely used in VLSI CAD tools.
- Student will be in a position to understand the changes introduced in the device models as

well as contribute to the development of appropriate device models.		

REFERENCES:

1. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly, Wayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd.
2. B. G. Streetman and S. Banarjee, "Solid State Electronic Devices", Prentice-Hall of India Pvt. Ltd, New Delhi, India.
3. A. B. Bhattacharyya, "Compact MOSFET Models for VLSI Design", John Wiley & Sons Inc., 2009.

AL18015	TESTING OF VLSI CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- The present course will introduce the student to the mathematical and scientific principles based on which systematic test and validation can be carried out on multimillion transistor VLSI design.

UNIT I	**BASICS OF TESTING AND FAULT MODELLING**	**9**

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.

UNIT II	**TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS**	**9**

Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits.

UNIT III	**DESIGN FOR TESTABILITY**	**9**

Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches.

UNIT IV	**SELF-TEST AND TEST ALGORITHMS**	**9**

Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

UNIT V	**FAULT DIAGNOSIS**	**9**

Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- The student who completes this course will be familiar with the principles used in the construction VLSI Design For Test (DFT) tools.
- The student will be able to adapt these to his specific industrial needs, also
- contribute to the development of more efficient tools from the fault overage and speed point of view.

REFERENCES:

1.L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.

AL18016	VLSI SIGNAL PROCESSING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I	**INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS**	**9**

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II	**RETIMING, ALGORITHMIC STRENGTH REDUCTION**	**9**

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III	**FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS**	**9**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV	**BIT-LEVEL ARITHMETIC ARCHITECTURES**	**9**

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.

UNIT V	**NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING**	**9**

Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- Ability to modify the existing or new DSP architectures suitable for VLSI Implementation

REFERENCES:		
1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007. 2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004		

AL18017	CAD FOR VLSI CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- The design of all VLSI circuits is carried out by making extensive use Computer Aided Design (CAD) VLSI design tool. Due to continuous scaling of semiconductor technology, most of the VLSI designs employ millions of transistors and circuits of this size can only be carried out with the aid of CAD VLSI design tools.
- The VLSI design professional needs to have a good understanding of the operation of these CAD VLSI design tools as these are developed primarily for and by the VLSI design professionals.
- As part of the present introductory course the principles of operation of all the important modules that go into the construction of a complete VLSI CAD tool will be discussed. These include the design flow organization for VLSI, the standard cell based synthesis methodologies for digital VLSI, floor planning and placement principles and related topics will be covered

UNIT I	**VLSI DESIGN METHODOLOGIES**	**9**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II	**DESIGN RULES**	**9**

Layout Compaction - Design rules problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation Placement algorithms-partitioning

UNIT III	**FLOOR PLANNING**	**9**

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV	**SIMULATION**	**9**

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V	**MODELLING AND SYNTHESIS**	**9**

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TOTAL: (L: + T:) : 45 PERIODS

OUTCOMES:

- Use VLSI design automation tools
- Perform high level synthesis
- Discuss floor planning concepts
- Design algorithms for placement and partitioning

REFERENCES:

1.S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
2.N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

AL18018	DSP INTEGRATED CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To familiarize the concept of DSP and DSP algorithms.
- Introduction to Multirate systems and finite wordlength effects
- To know about the basic DSP processor architectures and the synthesis of the processing elements
- To gather an idea about the VLSI circuit layout design styles

UNIT I	**INTRODUCTION TO DSP INTEGRATED CIRCUITS**	**9**

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific IC‟s for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT II	**DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS**	**9**

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT III	**DSP ARCHITECTURES**	**9**

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. TMS320C54x and TMS320C6x architecture, Motorola DSP56002 architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures.

UNIT IV	**SYNTHESIS OF DSP ARCHITECTURES AND ARITHMETIC UNIT**	**9**

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

Arithmetic Unit : Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator.

UNIT V	**CASE STUDY-INTEGRATED CIRCUIT DESIGN**	**9**

Layout of VLSI circuits, Layout Styles, Case Study : FFT processor, DCT processor and Interpolator.

TOTAL: (L: + T:): 45 PERIODS

OUTCOMES:

- Get to know about the Digital Signal Processing concepts and it‟s algorithms
- Get an idea about finite wordlength effects in digital filters

- Concept behind multirate systems is understood.
- Get familiar with the DSP processor architectures and how to perform synthesis of processing elements
- Acquire an general idea about VLSI circuit layout design aspects

REFERENCES:

1. Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York, 1999.
2. John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", PearsonEducation, 2002.
3. B.Venkatramani, M.Bhaskar, "Digital Signal Processors", Tata McGraw-Hill, 2002.
4. Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital signal processing – A practical approach", Tata McGraw-Hill, 2002.
5. Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.

AL18019	ADVANCED DIGITAL IMAGE PROCESSING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the image fundamentals.
- To understand the various image segmentation techniques.
- To extract features for image analysis.
- To introduce the concepts of image registration and image fusion.
- To illustrate 3D image visualization.

UNIT I	**FUNDAMENTALS OF DIGITAL IMAGE PROCESSING**	**9**

Elements of visual perception, brightness, contrast, hue, saturation, mach band effect, 2D image transforms-DFT, DCT, KLT,SVD. Image enhancement in spatial and frequency domain, Review of Morphological image processing.

UNIT II	**SEGMENTATION**	**9**

Edge detection, Thresholding, Region growing, Fuzzy clustering, Watershed algorithm, Active contour models, Texture feature based segmentation, Graph based segmentation, Wavelet based Segmentation - Applications of image segmentation.

UNIT III	**FEATURE EXTRACTION**	**9**

First and second order edge detection operators, Phase congruency, Localized feature extraction - detecting image curvature, shape features, Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors- Autocorrelation, Co-occurrence features, Runlength features, Fractal model based features, Gabor filter, wavelet features.

UNIT IV	**REGISTRATION AND IMAGE FUSION**	**9**

Registration - Preprocessing, Feature selection - points, lines, regions and templates Feature correspondence - Point pattern matching, Line matching, Region matching, Template matching. Transformation functions - Similarity transformation and Affine Transformation. Resampling – Nearest Neighbour and Cubic Splines. Image Fusion - Overview of image fusion, pixel fusion, wavelet based fusion -region based fusion.

UNIT V	**3D IMAGE VISUALIZATION**	**9**

Sources of 3D Data sets, Slicing the Data set, Arbitrary section planes, The use of color, Volumetric display, Stereo Viewing, Ray tracing, Reflection, Surfaces, Multiple connected surfaces, Image processing in 3D, Measurements on 3D images.

TOTAL : 45 PERIODS

OUTCOMES: At the end of the course, the student should be able to:

- Explain the fundamentals digital image processing.
- Describe image various segmentation and feature extraction techniques for image analysis.
- Discuss the concepts of image registration and fusion.
- Explain 3D image visualization.

REFERENCES:	
1.	Ardeshir Goshtasby, " 2D and 3D Image registration for Medical, Remote Sensing and Industrial Applications",John Wiley and Sons,2005.
2.	Anil K. Jain, Fundamentals of Digital Image Processing', Pearson Education, Inc., 2002
3.	C.Russ, "The Image Processing Handbook", CRC Press,2007
4.	Mark Nixon, Alberto Aguado, "Feature Extraction and Image Processing", Academic Press,2008.
5.	Rafael C. Gonzalez, Richard E. Woods, Digital Image Processing', Pearson,Education, Inc.,Second Edition, 2004.
6.	Rick S.Blum, Zheng Liu, "Multisensor image fusion and its Applications", Taylor& Francis,2006.

CU18015	MOBILE AD HOC NETWORKS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introduce the characteristic features of adhoc wireless networks and their applications to the students.
- To enable the student to understand the functioning of different access and routing protocols that can be used for adhoc networks.
- To enable the student to understand the need for security and the challenges and also the role of crosslayer design in enhancing the network performance.

UNIT I	**INTRODUCTION**	**9**

Introduction to Ad Hoc networks – definition, characteristics features, applications. Characteristics of Wireless channel, Adhoc Mobility Models: - entity and group models.

UNIT II	**MEDIUM ACCESS PROTOCOLS**	**9**

MAC Protocols: design issues, goals and classification. Contention based protocols, reservation based protocols, scheduling algorithms, protocols using directional antennas. IEEE standards: 802.11a, 802.11b, 802.11g, 802.15. HIPERLAN.

UNIT III	**NETWORK PROTOCOLS**	**9**

Addressing issues in ad hoc network, Routing Protocols: Design issues, goals and classification. Proactive Vs reactive routing, Unicast routing algorithms, Multicast routing algorithms, hybrid routing algorithm, Power/ Energy aware routing algorithm, Hierarchical Routing, QoS aware routing.

UNIT IV	**END -TO - END DELIVERY AND SECURITY**	**9**

Transport layer: Issues in designing- Transport layer classification, adhoc transport protocols. Security issues in adhoc networks: issues and challenges, network security attacks, secure routing protocols.

UNIT V	**CROSS LAYER DESIGN AND INTEGRATION**	**9**

Design of a wireless network and a wired network, prototype implementation to be simulated in a network simulator.

TOTAL : 45 PERIODS

OUTCOMES:At the end of the course, the student should be able to:

- The student would be able to demonstrate an understanding of the trade-offs involved in the design of adhoc networks
- The student would be able to design and implement protocols suitable to adhoc communication scenario using design tools and characterize them.
- The student is exposed to the advances in adhoc network design concepts.

REFERENCES:

1. C.Siva Ram Murthy and B.S.Manoj, ―Ad hoc Wireless Networks Architectures and protocols,2nd edition, Pearson Education. 2007
2. Charles E. Perkins, ―Ad hoc Networking, Addison – Wesley, 2000
3. Stefano Basagni, Marco Conti, Silvia Giordano and Ivan stojmenovic, ―Mobile adhoc networking, Wiley-IEEE press, 2004.

4.	Mohammad Ilyas, ―The handbook of adhoc wireless networks, CRC press, 2002.
5.	T. Camp, J. Boleng, and V. Davies ―A Survey of Mobility Models for Ad Hoc Network Research,Wireless Communication and Mobile Comp., Special Issue on Mobile Ad Hoc Networking Research, Trends and Applications, vol. 2, no. 5, 2002, pp. 483–502.
6.	Fekri M. Abduljalil and Shrikant K. Bodhe , ―A survey of integrating IP mobility protocols and Mobile Ad hoc networks, IEEE communication Survey and tutorials, v 9.no.1 2007.
7.	Erdal Çayırcı and Chunming Rong c, ― Security in Wireless Ad Hoc and Sensor Networks 2009, John Wiley & Sons, Ltd. ISBN: 978-0-470-02748-6

AL18311 & AL18411	PROJECT WORK PHASE I & II	L	T	P	C
		0	0	12	6
		0	0	24	12

OBJECTIVES:

- To make the student to take up an research issue related to communication system and provide an optimal solution for the same.
- To make the student to prepare a detailed report on the research issue they came across.

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent
need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following

- Relevance to social needs of society
- Relevance to value addition to existing facilities in the institute
- Relevance to industry need
- Problems of national importance
- Research and development in various domain

The student should complete the following:

- Literature survey Problem Definition
- Motivation for study and Objectives
- Preliminary design / feasibility / modular approaches
- Implementation and Verification
- Report and presentation

The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on:

- Experimental verification / Proof of concept.
- Design, fabrication, testing of Communication System.
- The viva-voce examination will be based on the above report and work.

Guidelines for Dissertation Phase – I and II

- Dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June.
    - The dissertation may be carried out preferably in-house i.e. department's laboratories and

  centers OR in industry allotted through department's T & P coordinator.
    - After multiple interactions with guide and based on comprehensive literature survey, the

  student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems,Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.

  Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
    - Phase – I deliverables: A document report comprising of summary of literature survey,

  detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
- Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In

  case of unsatisfactory performance, committee may recommend repeating the Phase-I work.
    - During phase – II, student is expected to exert on design, development and testing of the

  proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences

  OR IP/Patents.
    - Phase – II deliverables: A dissertation report as per the specified format, developed system in

  the form of hardware and/or software, A record of continuous progress.
    - Phase – II evaluation: Guide along with appointed external examiner shall

  assess theprogress/performance of the student based on report, presentation and Q & A.
  In case ofun satisfactory performance, committee may recommend for extension or repeating

  the work

TOTAL : 12 + 24 = 36