SRI VENKATESWARA COLLEGE OF ENGINEERING

COURSE DELIVERY PLAN - THEORY

Department of Information Technology/Computer Science & Engineering	**LP: CS16201** **Rev. No: 00** **Date: 29/12/2016**
B.E/B.Tech/M.E/M.Tech : CS/IT Regulation:2016 **Sub. Code / Sub. Name : CS16201 - DIGITAL PRINCIPLES AND DESIGN** **Unit : I**	

UNIT-I BOOLEAN ALGEBRA AND LOGIC GATES

Syllabus: Review of Number Systems – Arithmetic Operations – Binary Codes – Boolean Algebra and Theorems – Boolean Functions – Simplification of Boolean Functions using Karnaugh Map and Tabulation Methods – Logic Gates – NAND and NOR Implementations.

Objective: To understand various number systems, different methods used for the simplification of Boolean functions & logic gates

Session No *	Topics to be covered	Ref	Teaching Aids
1	Review of Number Systems, Binary Codes	T1-Ch-1 Pg 1-13	BB/LCD
2	Arithmetic Operations & Binary Codes	T1-Ch-1 Pg 13-16	BB/LCD
3	Boolean Algebra and Theorems	T1-Ch-2 Pg 34-41	BB/LCD
4	Boolean Functions	T1-Ch-2 Pg 42-45 R1-Ch-4 Pg 184-198	BB/LCD
5	Simplification of Boolean Functions using Karnaugh Map	T1-Ch-2 Pg 45-66 R1-Ch-4 Pg 205-223 R2-Ch-5 Pg 123-153	BB/LCD
6	Simplification of Boolean Functions using Karnaugh Map	T1-Ch-3 Pg 67-86 R1-Ch-4 Pg 205-223	BB/LCD
7	Simplification of Boolean Functions using Tabulation Methods	T1-Ch-3 Pg -112-120	BB/LCD
8	Simplification of Boolean Functions using Tabulation Methods	T1-Ch-3 Pg 112-120	BB/LCD
9	Logic Gates – NAND and NOR Implementations	T1-Ch-3 Pg 87-119	BB/LCD
10	Boolean Functions – NAND and NOR Implementations	T1-Ch-3 Pg 87-119	BB/LCD
Content beyond syllabus covered (if any):			

* Session duration: 50 minutes

Sub. Code / Sub. Name: CS16201 - DIGITAL PRINCIPLES AND DESIGN
Unit : II

UNIT - II COMBINATIONAL CIRCUITS

Syllabus: Combinational Circuits – Analysis and Design Procedures – Circuits for Arithmetic Operations, Code Conversion – Decoders and Encoders – Multiplexers and De multiplexers – Introduction to HDL – HDL Models of Combinational circuits**.**

Objective: To design and implement a system that uses combinational logic for the given specification; Simulate combinational logic systems using verilog or VHDL.

Session No *	Topics to be covered	Ref	Teaching Aids
11	Combinational Logic Introduction	T1-Ch-4 Pg 135-135 R1 Ch 4 Pg 184-198	BB/LCD
12	Combinational Circuits - Analysis and Design Procedures	T1-Ch-4 Pg 136-142 R1 Ch 4 Pg 199-223	BB/LCD
13	Circuits for Arithmetic Operations-Binary adder-Subtractor, Decimal Adder	T1-Ch-4 Pg 143-154 R5	BB/LCD
14	Circuits for Arithmetic Operations-Binary Multiplier, Magnitude comparator	T1-Ch-4 Pg 155-161 R5	BB/LCD
15	Code Conversion	T1-Ch-4 Pg 301-314 R6	BB/LCD
16	Decoders and Encoders	T1-Ch-4 Pg 162-167 R7	BB/LCD
17	Multiplexers	T1-Ch-4 Pg 168-173 R8	BB/LCD
18	Introduction to HDL HDL Models of Combinational circuits	T1-Ch4 Pg 174-188 R1 Ch 5 Pg 238-242	LCD
Content beyond syllabus covered (if any):			

* Session duration: 50 mins

Sub. Code / Sub. Name: : CS16201 - DIGITAL PRINCIPLES AND DESIGN
Unit : III

UNIT- III SYNCHRONOUS SEQUENTIAL LOGIC

Syllabus: Sequential Circuits – Latches and Flip Flops – Analysis and Design Procedures – State Reduction and State Assignment – Shift Registers – Counters – HDL for Sequential Logic Circuits.

Objective: To design and implement synchronous sequential system for the given specification; Simulate sequential logic systems using verilog or VHDL

Session No *	Topics to be covered	Ref	Teaching Aids
19	Sequential Circuits – Introduction	T1-Ch-5 Pg 197-198	BB/LCD
20	Latches and Flip Flops	T1-Ch-5 Pg 199-209 R1-Ch 7 Pg 526-541 R2-Ch 11 Pg 332	BB/LCD
21	Sequential Circuits-Analysis and Design Procedure	T1-Ch-5 Pg 210-220 R1-Ch 7 Pg 542-552	BB/LCD
22	State Reduction and State Assignment	T1-Ch-5 Pg 233-237 R1-Ch 7 Pg 553-569	BB/LCD
23	State Reduction and State Assignment	T1-Ch-5 Pg 233-237 R1-Ch 7 Pg 553-569	BB/LCD
24	Shift Registers-INTRODUCTION	T1-Ch-6 Pg 253-254 R1 Ch 8 Pg 727-755	BB/LCD
25	Shift Registers	T1-Ch-6 Pg 255-267 R1 Ch 8 Pg 727-755	BB/LCD
26	Counters-ripple Counters	T1-Ch-6 Pg 268-281 R1 Ch 8 Pg 710-711	BB/LCD
27	Counters-Synchronous and Other counters	T1-Ch-6 Pg 282-292 R1 Ch 8 Pg 711-712	LCD
28	HDL for Sequential Logic Circuits-Synthesizable HDL models of Sequential Circuits	T1-Ch 5 Pg 221-232,293-297	LCD
Content beyond syllabus covered (if any):			

* Session duration: 50 mins

Sub. Code / Sub. Name: CS16201 - DIGITAL PRINCIPLES AND DESIGN
Unit : IV

UNIT IV ASYNCHRONOUS SEQUENTIAL LOGIC

Syllabus: Analysis and Design of Asynchronous Sequential Circuits – Reduction of State and Flow Tables – Race-free State Assignment – Hazards.

Objective: To design and implement Asynchronous sequential system for the given specification.

Session No *	Topics to be covered	Ref	Teaching Aids
29	Asynchronous Sequential Circuits- Introduction	T1-Ch-9 Pg 355-435	BB/LCD
30	Analysis Procedure	T1-Ch-9 Pg 436-442 R3-Ch-9 Pg 505-519	BB/LCD
31	Circuits with Latches	T1-Ch-9 Pg 443-450	BB/LCD
32	Design of Asynchronous Sequential Circuits	T1-Ch-9 Pg 451-456 R3-Ch-9 Pg 505-519	BB/LCD
33	Reduction of State and Flow Tables	T1-Ch-9 Pg 457-463	BB/LCD
34	Race-free State Assignment	T1-Ch-9 Pg 464-468 R3-Ch-9 Pg 520	BB/LCD
35	Hazards	T1-Ch-9 Pg 469-473	BB/LCD
Content beyond syllabus covered (if any):			

* Session duration: 50 mins

Sub. Code / Sub. Name: CS16201 - DIGITAL PRINCIPLES AND DESIGN
Unit : V

UNIT V MEMORY AND PROGRAMMABLE LOGIC

Syllabus: RAM and ROM – Memory Decoding – Error Detection and Correction – Programmable Logic Array – Programmable Array Logic – Sequential Programmable Devices – Application Specific Integrated Circuits.

Objective: To design and implement memory accessing systems and systems using PLD

Session No *	Topics to be covered	Ref	Teaching Aids
36	Memory and Programmable logic Introduction	T1-Ch 7 Pg 307	BB/LCD
37	RAM – Memory Decoding	T1-Ch 7 Pg 308-313 R1- Ch 9 Pg 822-839	BB/LCD
38	Memory Decoding	T1-Ch 7 Pg 314-318	BB/LCD
39	Error Detection and Correction	T1-Ch 7 Pg 319-321	BB/LCD
40	ROM	T1-Ch 7 Pg 322-327 R1- Ch 9 Pg 800-820	BB/LCD
41	Programmable Logic Array	T1-Ch 7 Pg 328-331	BB/LCD
42	Programmable Logic Array	T1-Ch 7 Pg 328-331	BB/LCD
43	Programmable Array Logic	T1-Ch 7 Pg 332-335	BB/LCD
44	Sequential Programmable Devices	T1-Ch 7 Pg 336-350	BB/LCD
45	Application Specific Integrated Circuits	Internet	LCD

* Session duration: 50 mins

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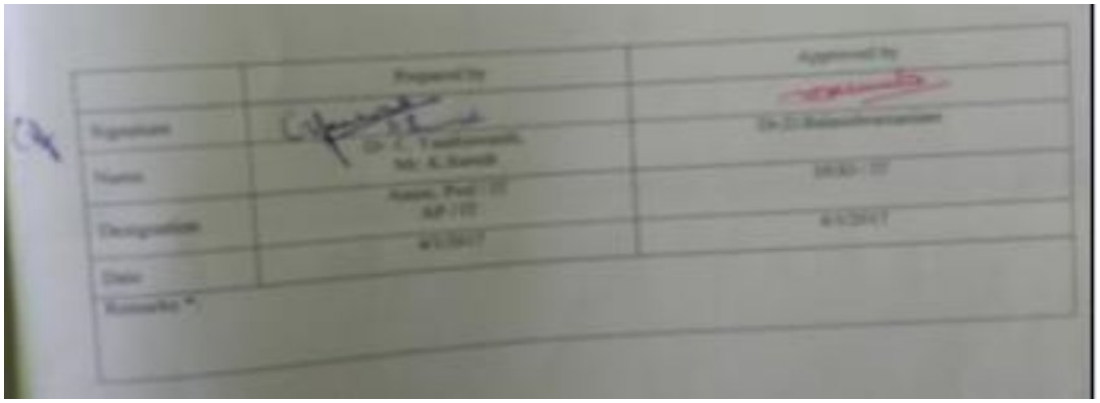
TEXT BOOK:

1. Morris Mano M. and Michael D. Ciletti, “Digital Design”, IV Edition, Pearson Education, 2008.

REFERENCES:

1. John F. Wakerly, “Digital Design Principles and Practices”, Fourth Edition, Pearson Education,2007.
2. Charles H. Roth Jr, “Fundamentals of Logic Design”, Fifth Edition – Jaico Publishing House, Mumbai, 2003.
3. Donald D. Givone, “Digital Principles and Design”, Tata Mcgraw Hill, 2003.
4.Kharate G. K., “Digital Electronics”, Oxford University Press, 2010.



* If the same lesson