SRI VENKATESWARA COLLEGE OF ENGINEERING

COURSE DELIVERY PLAN - THEORY

Department of Information Technology	
B.Tech: IT **Sub. Code / Sub. Name: IT16301 - Computer Organization and Architecture** **Regulation:2016** **Unit : I**	**LP: IT16301** **Rev. No: 00** **Date: 23/06/2017**

UNIT-I BASIC COMPUTER ORGANIZATION AND DESIGN

Syllabus: Instruction codes, Computer registers, computer instructions, Timing and Control, Instruction cycle, Memory-Reference Instructions, Input-output and interrupt, Complete computer description, Design of Basic computer, design of Accumulator Unit. Register Transfer Language, Register transfer, Bus and Memory transfer, Arithmetic Micro-operations, Logic Micro-operations, Shift –Micro operations, Arithmetic Logic Shift

Objective: To understand the basic structure and operations of digital computer and the hardware-software interface

Session No *	Topics to be covered	Ref	Teaching Aids
1	Instruction codes – Stored Program Organization -Indirect Address, Computer registers – Common Bus System	T1, Ch.5 (Pg.no.123-132)	BB/LCD
2	Computer Instructions – Instruction Set Completeness, Timing and Control	T1, Ch.5 (Pg.no.132-139)	BB/LCD
3	Instruction cycle – Fetch and Decode - Determine the type of Instructions – Register Reference Instructions, Memory-Reference Instructions	T1, Ch.5 (Pg.no.139-150)	BB/LCD
4	Input-Output and interrupt - Input-Output Configuration - Input-Output Instructions – Program Interrupt, Complete computer description	T1, Ch.5 (Pg.no.150-157)	BB/LCD
5	Design of Basic computer, Design of Accumulator Unit	T1, Ch.5 (Pg.no.157-167)	BB/LCD
6	Register Transfer Language, Register transfer, Bus and Memory transfer	T1, Ch.4 (Pg.no.93-102)	BB/LCD
7	Arithmetic Micro-operations	T1, Ch.4 (Pg.no.102-108)	BB/LCD
8	Logic Micro-operations	T1, Ch.4 (Pg.no.108-114)	BB/LCD
9	Shift -Microoperations, Arithmatic Logic Shift	T1, Ch.4 (Pg.no.114-119)	BB/LCD
Content beyond syllabus covered (if any):Nil			

* Session duration: 50 minutes

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Sub. Code / Sub. Name: IT16301 - Computer Organization and Architecture
Unit : II

UNIT - II ALU AND CU

Syllabus: ALU - Addition and subtraction – Multiplication – Division – Floating Point operations – Sub word parallelism. CPU- General Register Organization, Stack Organization, Instruction format, Addressing Modes, data transfer and manipulation, Program Control, Reduced Instruction Set Computer (RISC).

Objective: To familiarize with arithmetic and logic unit and implementation of fixed point and floating point arithmetic operations.

Session No *	Topics to be covered	Ref	Teaching Aids
10	ALU - Addition and subtraction	T2, Ch.3 (Pg.no.176-183)	BB/LCD
11	Multiplication, Division	T2, Ch.3 (Pg.no.183-196)	BB/LCD
12	Floating Point operations	T2, Ch.3 (Pg.no.196-222)	BB/LCD
13	Sub word parallelism	T2, Ch.3 (Pg.no.222-224)	BB/LCD
14	CPU- General Register Organization	T1, Ch.8 (Pg.no.243-249)	BB/LCD
15	Stack Organization	T1, Ch.8 (Pg.no.249-257)	BB/LCD
16	Instruction format, Addressing Modes	T1, Ch.8 (Pg.no.257-268)	BB/LCD
17	Data transfer and manipulation, Program Control	T1, Ch.8 (Pg.no.268-284)	BB/LCD
18	Reduced Instruction Set Computer (RISC)	T1, Ch.8 (Pg.no.284-293)	BB/LCD
Content beyond syllabus covered (if any):Nil			

* Session duration: 50 mins

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Sub. Code / Sub. Name: IT16301 - Computer Organization and Architecture
Unit : III

UNIT- III PROCESSOR

Syllabus: Basic MIPS implementation – Building datapath – Control Implementation scheme – Pipelining – Pipelined datapath and control – Handling Data hazards & Control hazards – Exceptions, The ARM Cortex-A8 and Intel Core i7 Pipelines.

Objective: To differentiate various data path and control schemes and to handle data hazards and control hazards.

Session No *	Topics to be covered	Ref	Teaching Aids
19	Basic MIPS implementation- An overview of the implementation, Logic design conventions.	T2,Ch.4(Pg.no.244-251,) T2,Ch.B(Pg.no.B3-B10)	BB/LCD
20	Building a datapath, creating a single data path, Example for building a data path	T2,Ch.4(Pg.no.251-259), R3,Ch.4(Pg.no.479-481), R5,Ch.5(Pg.no.150-162)	BB/LCD
21	Control implementation scheme – The ALU control, Designing the control unit, operation of the data path	T2,Ch.4(Pg.no.259-269), R5,Ch.5(Pg.no.163-171)	BB/LCD
22	Finalizing Control, example for Implementing Jumps, Why a Single-Cycle Implementation Is Not Used Today	T2,Ch.4(Pg.no.269-272)	BB/LCD
23	Pipelining-An overview of pipelining, designing instruction sets for pipelining, pipeline hazards, structural hazards, data hazards. A pipelined data path, graphically representing pipelines.	T2,Ch.4(Pg.no.272-286), R5,Ch.5(Pg.no.195-227), R7,Ch.5(Pg.no.275-292) T2,Ch.4(Pg.no.286-300),	BB/LCD
24	Pipelined control, separation of control lines according to pipeline stage	T2,Ch.4(Pg.no.300-303)	BB/LCD
25	Data hazards: Forwarding versus Stalling, Dependence detection	T2,Ch.4(Pg.no.303-312), R3,Ch.4(Pg.no.461-464)	BB/LCD
26	Data hazards and stalls, Control hazards, Assume branch not taken, Reducing the delay of branches, Pipelined branch example. Dynamic branch prediction, Example for Loops and prediction,	T2,Ch.4(Pg.no.313-320), R3,Ch.4(Pg.no.465-470), T2,Ch.4(Pg.no.321-325)	BB/LCD
27	Exceptions- How Exceptions Are Handled in the MIPS Architecture Exceptions in a Pipelined Implementation, Exception in a Pipelined Computer example Branch hazards. The ARM Cortex -A8 and Intel Core i7 pipelines	T2,Ch.4(Pg.no.326-332) T2,Ch.4(Pg.no.344-350)	BB/LCD

Content beyond syllabus covered (if any):

* Session duration: 50 mins

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Sub. Code / Sub. Name: IT16301 - Computer Organization and Architecture
Unit : IV

UNIT IV MEMORY AND I/O SYSTEMS

Syllabus: Memory hierarchy - Memory technologies - Cache basics - Measuring and improving cache performance - Virtual memory, TLBs - Input/output system, programmed I/O, DMA and interrupts, I/O processors.

Objective: To measure and improve the cache performance by understanding various memory technologies

Session No *	Topics to be covered	Ref	Teaching Aids
28	Memory hierarchy design - Introduction, Basics of Memory Hierarchies: An quick review	T2,Ch.5(Pg.no.374-378), R5,Ch.12(Pg.no.344-349)	BB/LCD
29	Memory technology and Optimizations, SRAM Technology, DRAM technology, Improving memory performance inside a DRAM chip	T2,Ch.5(Pg.no.378-383), R7,Ch.9(Pg.no.400-425)	BB/LCD
30	The Basics of Caches, Accessing a Cache, Handling Cache Misses, Handling Writes, Designing the Memory System to Support Caches	T2,Ch.5(Pg.no.383-398), R4,Ch.4(Pg.no.110-140), R5,Ch.12(Pg.no.349-358)	BB/LCD
31	Measuring and Improving Cache Performance, Calculating Cache Performance and Average Memory Access Time, Locating a Block in the Cache, Reducing the Miss Penalty Using Multilevel Caches	T2,Ch.5(Pg.no.398-418)	BB/LCD
32	Virtual memory, Placing a Page and Finding It Again, Page Faults, Integrating Virtual Memory, TLBs, and Caches, Implementing Protection with Virtual Memory, Handling TLB Misses and Page Faults	T2,Ch.5(Pg.no.427-454), R3,Ch.8(Pg.no.337-342), R5,Ch.12(Pg.no.358-370)	BB/LCD
33	Input/output system	R5,Ch.12(Pg.no.377-380)	BB/LCD
34	programmed I/O	R4,Ch.4(Pg.no.224-228), R5,Ch.12(Pg.no.380-391), R7,Ch.987(Pg.no.504-511)	BB/LCD
35	DMA and interrupts	R4,Ch.4(Pg.no.228-242), R5,Ch.12(Pg.no.391-401), R7,Ch.9(Pg.no.511-523)	BB/LCD
36	I/O processors	R4,Ch.4(Pg.no.242-253), R7,Ch.9(Pg.no.523-529)	BB/LCD
Content beyond syllabus covered (if any):			

* Session duration: 50 mins

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Sub. Code / Sub. Name: IT16301 - Computer Organization and Architecture
Unit : V

UNIT V MULTICORES, MULTIPROCESSORS, AND CLUSTERS

Syllabus: Shared Memory Multiprocessors, Clusters and Other Message-Passing Multiprocessors Hardware Multithreading, SISD, MIMD, SIMD, SPMD, and Vector, Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers, and Other Message-Passing Multiprocessors

Objective: To classify between SISD,MIMD,SIMD,SPMD and various warehouse scale computers.

Session No *	Topics to be covered	Ref	Teaching Aids
37	Shared Memory Multiprocessors	T2,Ch.6(Pg.no.638-640)	BB/LCD
38	Clusters and other message-passing multiprocessors	T2,Ch.6(Pg.no.641-645)	BB/LCD
39	Hardware Multithreading	T2,Ch.6(Pg.no.645-648)	BB/LCD
40	SIMD,MIMD,SIMD,SPMD - SIMD in x86: Multimedia Extensions	T2,Ch.6(Pg.no.648-650)	BB/LCD
41	Vector-vector versus scalar-vector versus multimedia extensions	T2,Ch.6(Pg.no.650-653)	BB/LCD
42	Introduction to Graphics processing units	T2,Ch.6(Pg.no.654-660)	BB/LCD
43	Clusters- Warehouse scale computers and other message passing- Passing multiprocessors	T2,Ch.6(Pg.no.531-535)	BB/LCD
44	Introduction to Multiprocessor Network Topologies	T2,Ch.6(Pg.no.536-538)	BB/LCD
45	Multiprocessor Benchmarks and Performance Models	T2,Ch.6(Pg.no.540-549)	BB/LCD
Content beyond syllabus covered (if any): Introduction to Multiprocessor Network Topologies, Multiprocessor Benchmarks and Performance Models			

* Session duration: 50 mins

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Text Books:

1. M. Moris Mano, " Computer System Architecture", 3rd Edition, Pearson/ PHI, 2007
2. David A. Patterson and John L. Hennessey, "Computer organization and design□, Morgan kauffman / elsevier, Fifth edition, 2014.

References:

3. V. Carl Hamacher, Zvonko G. Varanesic and Safat G. Zaky, "Computer Organisation", VI edition, McGraw-Hill Inc, 2012.
4. William Stallings "Computer Organization and Architecture", Seventh Edition, Pearson Education, 2006.
5. Vincent P. Heuring, Harry F. Jordan, "Computer System Architecture", Second Edition, Pearson Education, 2005.
6. Govindarajalu, "Computer Architecture and Organization, Design Principles and Applications", first edition, Tata McGraw Hill, New Delhi, 2005.
7. John P. Hayes, "Computer Architecture and Organization", Third Edition, Tata McGraw Hill, 1998.
8. http://nptel.ac.in/.

	Prepared by	Approved by
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Name	N. Uma	Dr. V. Vidhya
Designation	Assistant Professor	Professor and Head
Date	23/06/2017	23/06/2017
Remarks *:		
Remarks *:		

* If the same lesson plan is followed in the subsequent semester/year it should be mentioned and signed by the Faculty and the HOD

It was decided that the same lesson plan has to be followed for the upcoming semester (2018-2019) in the course commited meeting.

29/06/18

2/7/18