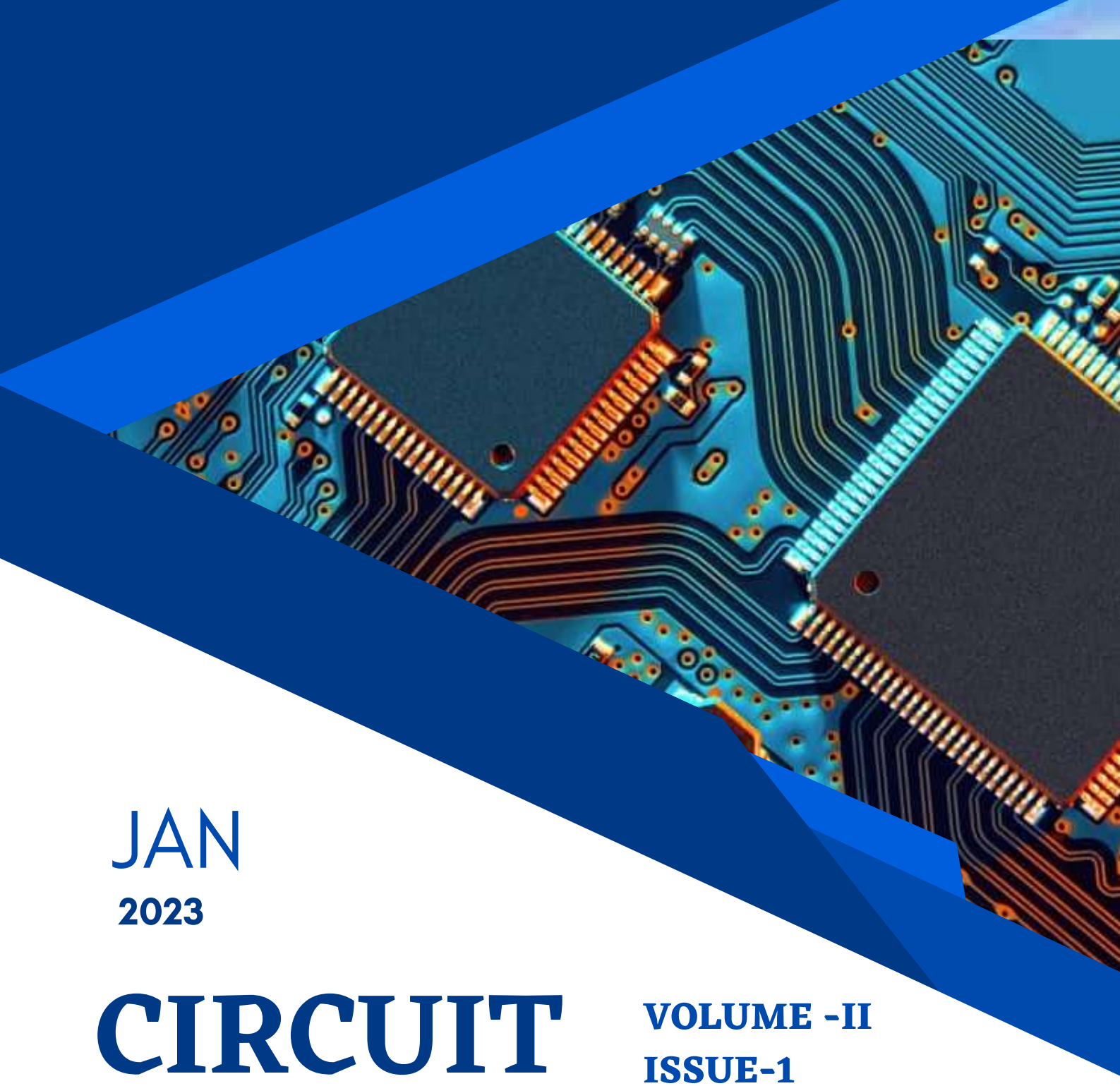

JAN
2023

CIRCUIT TIMES

VOLUME -II
ISSUE-1

SVCE | SRI VENKATESWARA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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VISION OF THE DEPARTMENT

To excel in offering value based quality education in the field of Electronics and Communication Engineering, keeping in pace with the latest developments in technology through exemplary research, to raise the intellectual competence to match global standards and to make significant contributions to the society.

MISSION OF THE DEPARTMENT

- To provide the best pedagogical atmosphere of highest quality through modern infrastructure, latest knowledge and cutting edge skills.
- To fulfill the research interests of faculty and students by promoting and sustaining in house research facilities so as to obtain the reputed publications and patents.
- To educate our students, the ethical and moral values, integrity, leadership and other quality aspects to cater to the growing need for values in the society.

Program Educational Objectives (PEOs)

PEO1: Create value to organizations as an EMPLOYEE at various levels, by improving the systems and processes using appropriate methods and tools learnt from the programme.

PEO2:Run an organization successfully with good social responsibility as an ENTREPRENEUR, making use of the knowledge and skills acquired from the programme.

PEO3:Contribute to the future by fostering research in the chosen area as an ERUDITE SCHOLAR, based on the motivation derived from the programme.

Program Specific Outcomes (PSOs)

PSO-1: An ability to apply the concepts of Electronics, Communications, Signal processing, VLSI, Control systems etc., in the design and implementation of application oriented engineering systems.

PSO-2: An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical and managerial skills to arrive appropriate solutions, either independently or in team.

ARTICLE

By Faculty

Artificial Intelligence and Machine Language Implementation in VLSI design Technology

S.R.Malathi, Professor, ECE

The horizons of Artificial Intelligence, Machine Learning, and Deep learning are no longer confined to the software domain. The major changes in software technology also creates the necessity for improved hardware. Machine Language is used by Artificial Intelligence Systems, that can self-learn without human intrusion based on the algorithm. Machine Learning and Deep Learning are applied to large data sets which involves multiple layers for data analysis. Smart behaviour of the systems requires considerable information to be absorbed. When new techniques in machine learning are being implemented, then new hardware systems and architectures will evolve rapidly to process the data in new ways.

Machine learning requires improved custom hardware to meet the developing designs. The systems and technologies developed are based on the Algorithms, Training Models, Rules etc. The software requires high-end hardware, which has remarkable computation capacity, consumes less power and can perform complex mathematical computations in fractions of microseconds.

Advancement in Technology

Electronics and Communication Engineering play a very important part in the evolution of the technology for AI systems. The development of AI has been supported by the advancements in chip technology, graphical processing units, sensors, communication networks, etc. The ever-growing VLSI technology and the upgradation from the design of VLSI chips to the Ultra Large Scale Integrated circuit systems has helped the AI systems to evolve. The integration of computer-aided design and program tools further improvised the computerization of VLSI design. The tools designed are capable of resolving diverse phases of the task design very proficiently. Artificial Intelligence techniques are amalgamated in VLSI design automation to tackle the issues of multiple design stages. For a problem statement, the ML models analyse multiple solutions and chooses the best possible solution.

These high data sets are dealt with Graphics Processing Units. It can be stated that the VLSI domain and Artificial Intelligence are co-dependent. Electronics has penetrated in wide range of applications such as cell phone, washing machine, microwave oven, AC, remote control, car electronics, aviation, weather forecast, spaceships, satellites, defence and everywhere.

There is a necessity for new electronic systems having low power consumption, higher battery backup, low cost, fastest computational speed, and very short design time. As the size of components is shrinking day by day, the study which is responsible for designing all these electronics needs modernization at a faster pace. The future will see a tremendous boost in the VLSI sector. To enhance the apparent growth in the nanometer range in the integrated circuit industry, it is necessary to reduce the turnaround time of chip manufacturing.

The exclusive strategies of artificial intelligence (AI) offer several exhilarating methods for handling complex and data-concentrated tasks in the design and testing for VLSI. The overall outcome enhances the Integrated circuit production while reducing the manufacturing turnaround time. The improvement in the overall turnaround time of a chip greatly depends upon the technology used in designing the system to overcome the overall design constraints.

An automated approach using the concepts of Artificial Intelligence and Machine Learning in VLSI design and manufacturing helps to transform the field of VLSI design to design high-velocity, highly intelligent, and efficient implementations.

Deep learning is a subsection of machine learning, which is in simple terms a neural network with more layers i.e., three or more. The role of these layers is to simulate the behaviour of the human brain. It trains the system from huge data sets. A single-layered network can only make estimated calculations. The more the number of layers, the more the efficiency can be enhanced. These hidden layers help to optimize and improve the accuracy. There are numerous day-to-day applications that use the concept of deep learning such as digital assistants, voice-enabled TV remotes, credit card fraud detection, self-driving cars, and many more.

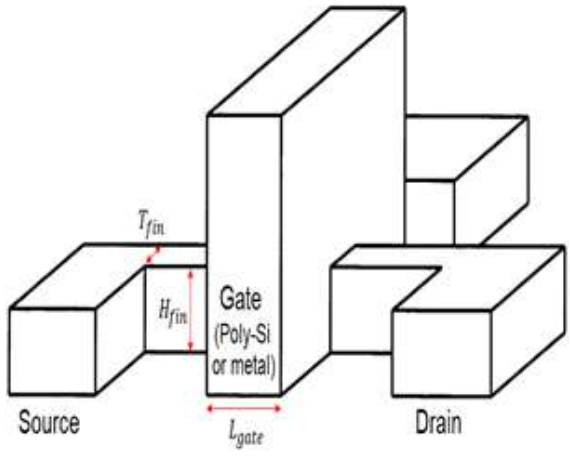
With the enhancement in the performance of the semiconductor design, the geometry of the transistor is shrinking and the technology is upgrading from basic transistors to non-planar FinFET devices. With the upcoming recent development of the graphic processor unit which is based on deep learning technology, the size of the device can be automated and controlled.

FinFET Technology

The semiconductor industry has been forced to reinvent fundamental transistor architecture and manufacturing processes due to continuous scaling of transistors. FinFET is the most advanced transistor that is currently commercially available. It is a type of multi-gate device for high speed/ high-density processors. Similar to the earlier generations of transistors, FinFET is hitting its limits in terms of scaling and leakage current, and it may need to be replaced with a new architecture in the near future.

The CMOS process currently dominates in PLDs and use less power than they did in decades past. Advanced technology in development will continue to be computationally intensive, and CMOS FinFETs are likely to remain the primary transistor architecture for these advanced applications. Every time the major semiconductor manufacturers scale to a new technology node, they need to reinvent the manufacturing process, transistor architecture, or both. The first commercially available products to use FinFETs were manufactured by Intel at the 22 nm node. The current commercialized transistor node is 7 nm.

FinFET technology was introduced after a gradual transition from planar architecture to a vertically-oriented gate architecture. FinFET technology simply completes the structure by enclosing the entire gate region with a wrap-around gate electrode. FinFET is often referred to as a “trigate”, as it surrounds the channel on 3 sides (out of 4 possible). In this structure, the gate electrode can be made from polysilicon or a metal alloy, and there is a thin insulator between the channel region and the gate electrode. This was traditionally an oxide layer (e.g., in MOSFETs), although high-k dielectrics are now being used to combat short-channel effects. FinFETs can also be formed with multiple fins placed in parallel, which gives larger gain with similar control over short-channel effects. Modern microprocessors, GPUs, and other high-density processors use FinFET technology as the fundamental transistor architecture.



FinFET Transistor Structure

The structure of a modern FinFET is shown below. In the structure shown, the source, gate, and drain can sit on an insulating layer (silicon on insulator, or SOI) or on bare silicon (bulk). SOI provides self-alignment during growth and strong isolation between neighbouring FinFET structures. Both SOI and bulk FinFETs can use metal or polysilicon gates.

Advantages of FinFETs

There are many reasons the industry has transitioned from 2D planar transistor architecture to other styles of transistors (including 3D FinFET transistors)—all of which centre around controlling leakage current. As transistors have scaled smaller, electrons have a higher probability of passing between the source and drain regions due to quantum tunnelling. This leads to higher leakage current when a source-drain voltage is applied, even if the gate is turned off. The wrap-around structure of a FinFET gives designers more control over leakage current.

Quantum Computing

Quantum computing is a rapidly-emerging technology that harnesses the laws of quantum mechanics to solve problems too complex for classical computers. Today, IBM Quantum makes real quantum hardware. Powerful superconducting quantum processor machines are very different from the classical computers.

When scientists and engineers encounter difficult problems, they turn to supercomputers. These are very large classical computers, often with thousands of classical CPU and GPU cores. However, even supercomputers struggle to solve certain kinds of problems with a high degree of complexity.

Complex problems are problems with lots of variables interacting in complicated ways. Modelling the behaviour of individual atoms in a molecule is a complex problem, because of all the different electrons interacting with one another. Sorting out the ideal routes for a few hundred tankers in a global shipping network is complex too. A supercomputer might be great at difficult tasks like sorting through a big database of protein sequences, but it will struggle to see the subtle patterns in that data that determine how those proteins behave.

Working of Quantum Computers

Quantum computers are elegant machines, smaller and requiring less energy than supercomputers. An IBM Quantum processor is a wafer not much bigger than the one found in a laptop. And a quantum hardware system is about the size of a car, made up mostly of cooling systems to keep the superconducting processor at its ultra-cold operational temperature.

A classical processor uses bits to perform its operations. A quantum computer uses qubits (CUE-bits) to run multidimensional quantum algorithms. The desktop computer uses a fan to get cold enough to work. Whereas the quantum processors need to be very cold – about a hundredth of a degree above absolute zero. To achieve this, super-cooled super-fluids are used to create superconductors. At those ultra-low temperatures certain materials in the processors exhibit another important quantum mechanical effect (i.e.) the electrons move through them without resistance. This makes them "superconductors."

When electrons pass through superconductors they match up, forming "Cooper pairs." These pairs can carry a charge across barriers, or insulators, through a process known as quantum tunnelling. Two superconductors placed on either side of an insulator form a Josephson junction. Josephson junctions are used as superconducting qubits. By firing microwave photons at these qubits, their behaviour can be controlled and get them to hold, change, and read out individual units of quantum information. A qubit itself isn't very useful. But it can perform an important trick by placing the quantum information it holds into a state of superposition, which represents a combination of all possible configurations of the qubit.

Groups of qubits in superposition can create complex, multidimensional computational spaces. Complex problems can be represented in new ways in these spaces.

Entanglement is a quantum mechanical effect that correlates the behaviour of two separate things. When two qubits are entangled, changes to one qubit directly impact the other. Quantum algorithms leverage those relationships to find solutions to complex problems But quantum advantage will not be achieved with hardware alone. IBM has developed the software that will be necessary to do useful work using quantum computers, the Qiskit quantum SDK. It is open-source, python-based, and the most widely-used quantum SDK in the world.

All this work is driving toward a future where quantum-centric supercomputers solve problems that are impossible to solve today, with near-term benefits to chemistry research.

ARTICLE

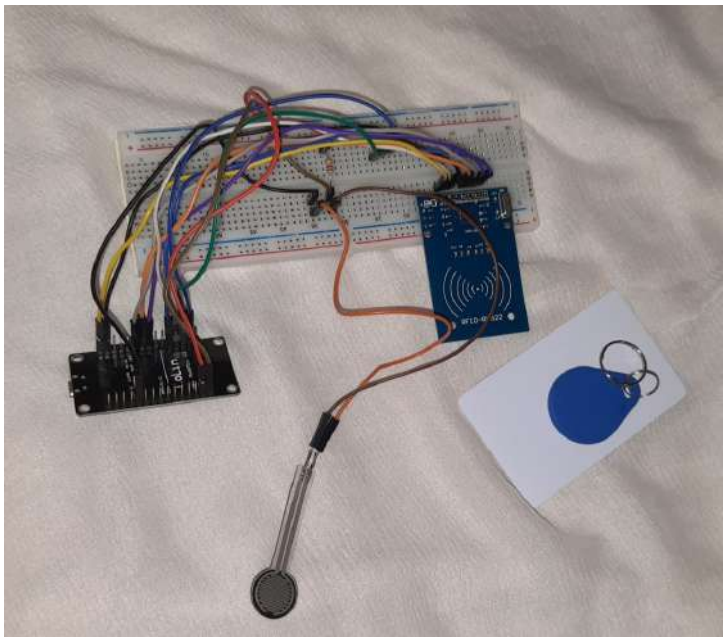
By Student

Smart Bus Ticketing System

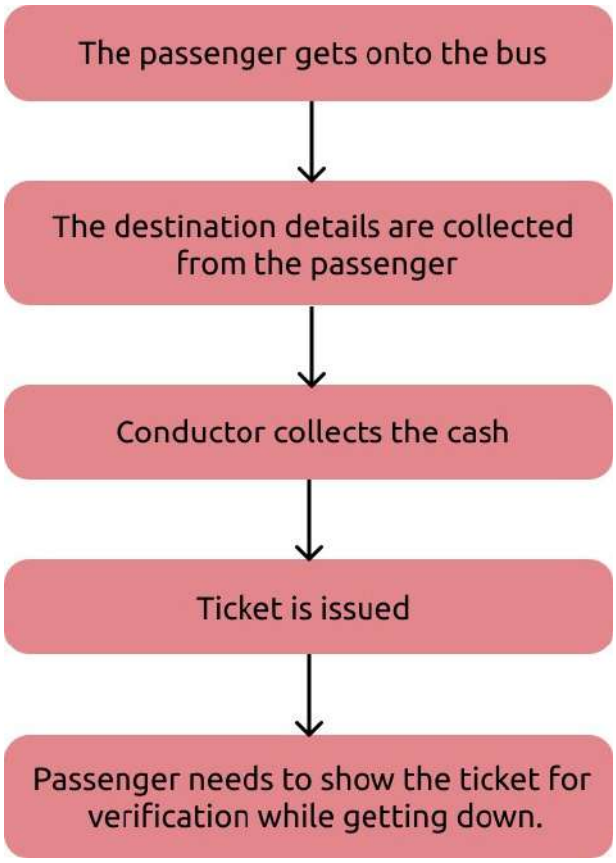
Rajit H and Srivani M, III year ECE

This work intends to replace every inconvenient means of purchasing public transportation tickets with a completely automated solution as simple as carrying a credit card-sized ID in your pocket. An app is developed to generate the ticket and notify the user who has just boarded the bus. The starting and ending places of the journey are to be provided by the passenger and the distance between the two points is determined before generating a suitable ticket.

Every time a passenger boards the bus, he or she must tap the RFID tag (the white cards or blue tags) on the RFID reader. As a result, the NodeMCU attached to the reader will detect the distinctive ID of the traveler's RFID tag and update credentials and starting location. As soon as a passenger sits down on the bus, the force sensors positioned beneath the seats will detect the reading and update the app to show that the seat associated with the force sensor that was engaged is "occupied."



Passengers must tap the RFID tag on the reader when they exit the vehicle. The position where the passenger exits are now updated in the database, and using the starting and ending coordinates, the trip's cost is calculated. The cost is then deducted from the passenger's balance amount that is maintained in the app.



If the balance is more than the trip cost, the cost is deducted from the balance; however, if the trip cost is higher than the balance, the overdue charges will be added to the person's account and the cost will be deducted from it the next time the balance is updated.

Here is a screenshot of the app that displays the distance traveled and the associated expense.

FACULTY PARTICIPATION

- Dr. G A Sathish Kumar, Dr. N. Kumaratharan, Dr.P.Jothilakshmi, Dr. S. R. Malathi, Dr.R.Gayathri, Professor and Dr. D.Menaka, Associate Professor attended AICTE Sponsored Workshop on " Gender Audits in Higher Education Institutions: The Why and How?" under the Distinguished Chair Professor Scheme on 27th and 28th January 2023.

- Dr. R. Priyadharshini attended Five Days Online Faculty Development Program (FDP) On Research Trends in Optical Technologies and its Applications (RTOTA-2023) organized by VIT University, Chennai Campus from 05-Jan-2023 to 09-Jan-2023.

- Dr. S. R. Malathi, Professor and Ms. S.M.Mehzabeen, participated in the “IP Awareness/ Training Program” under National Intellectual Property Awareness Mission (NIPAM) on 30-01-2023, organized by 'Intellectual Property Office, India' at SVCE

RESEARCH

BY FACULTY AND STUDENTS

The following research papers were published in journals by faculty and students during January 2023.

- Anju. L, Aniruddh Aiyengar, Tamil Selvan H, Vishnuvaradhan Moganarengam, "WEARABLE VIBRATION-BASED DEVICE FOR HEARING-IMPAIRED PEOPLE USING ACOUSTIC SCENE CLASSIFICATION", International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056 Volume: 10 Issue: 01 p-ISSN: 2395-0072

- S. Jayachitra, Dr.A. Prasanth, Shaik Mohammad Rafi, S. Zulaikha Beevi, Hierarchical-Based Binary Moth Flame Optimization for Feature Extraction in Biomedical Application, Proceedings of the International Conference on Machine Learning, Image Processing, Network Security and Data Sciences, pp.27-38, January 2023.

- Dr.P. Jothilakshmi, C. Gomatheeswari Preethika, R. Mohanasundaram, and Sagi. Sharvan Kumar, "Design of Reflectarray Unit Cell for Ku Band Satellite Communication," 2022 IEEE 6th Conference on Information and Communication Technology (CICT), Gwalior, India, 2022, pp. 1-6, doi: 10.1109/CICT56698.2022.9997910.

ACHIEVEMENTS

BY ALUMNI

- Mr. Pravin Shekar of 96 batch got the "Lifetime Achievement Award" From the PSAI - Professional Speakers Association India

- Mr. Rajit H, Ms.Srivani M, Ms. Sakthi Maheswari M of III year ECE won the third place in the 24hr hackathon conducted by FORESE and Coder's Forum.

BY STUDENTS

- Mr. Prithiviraj V S, Mr.Shivaganapathy R, Ms. Snehalatha M of III year ECE won the first place in the 24hr hackathon conducted by FORESE and Coder's Forum.

- SVCE Cricket Team showed a stunning performance and clinched the Winners title in Anna University Zonal Tournament which was organized from 10/01/2023 to 18/01/2023. Mr. ARVINDH.G from III year ECE is in the SVCE Cricket team.

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