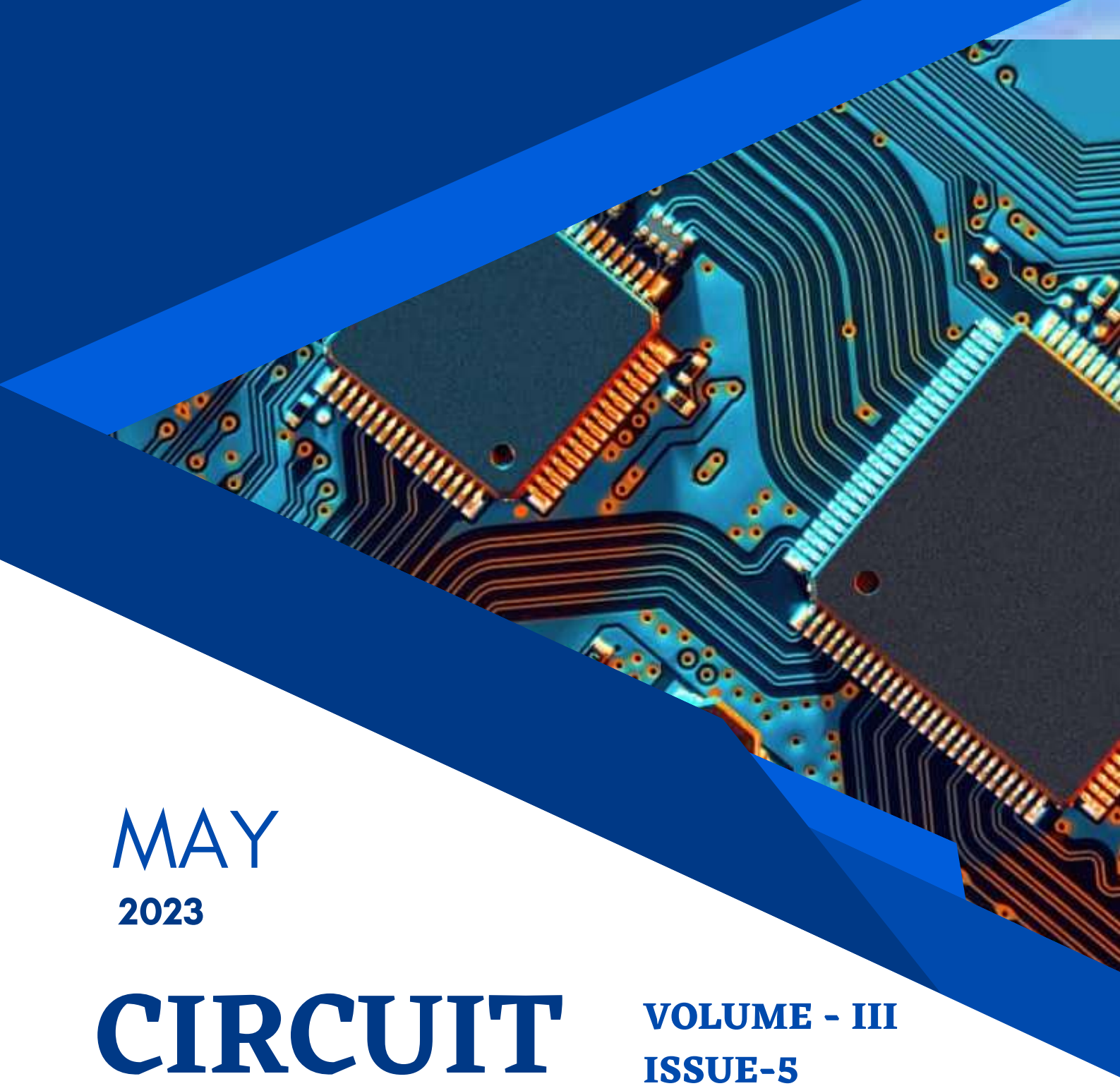

MAY
2023

CIRCUIT TIMES

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ISSUE-5

SVCE | SRI VENKATESWARA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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VISION OF THE DEPARTMENT

To excel in offering value based quality education in the field of Electronics and Communication Engineering, keeping in pace with the latest developments in technology through exemplary research, to raise the intellectual competence to match global standards and to make significant contributions to the society.

MISSION OF THE DEPARTMENT

- To provide the best pedagogical atmosphere of highest quality through modern infrastructure, latest knowledge and cutting edge skills.
- To fulfill the research interests of faculty and students by promoting and sustaining in house research facilities so as to obtain the reputed publications and patents.
- To educate our students, the ethical and moral values, integrity, leadership and other quality aspects to cater to the growing need for values in the society.

Program Educational Objectives (PEOs)

PEO1: Create value to organizations as an EMPLOYEE at various levels, by improving the systems and processes using appropriate methods and tools learnt from the programme.

PEO2:Run an organization successfully with good social responsibility as an ENTREPRENEUR, making use of the knowledge and skills acquired from the programme.

PEO3:Contribute to the future by fostering research in the chosen area as an ERUDITE SCHOLAR, based on the motivation derived from the programme.

Program Specific Outcomes (PSOs)

PSO-1: An ability to apply the concepts of Electronics, Communications, Signal processing, VLSI, Control systems etc., in the design and implementation of application oriented engineering systems.

PSO-2: An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical and managerial skills to arrive appropriate solutions, either independently or in team.

FACULTY ARTICLE

3D INTEGRATION IN VLSI CIRCUITS

Mr.M.Athappan, Associate Professor, Department of ECE, SVCE

Introduction

Field-programmable gate arrays (FPGAs) are playing a larger and more complicated role in system designs, which calls for better logic capacity as well as more on-chip resources and capabilities. FPGAs have largely relied on Moore's law scaling up until the 40 nm node to meet this need, providing approximately double the logic capacity with each successive process generation. However, Moore's law alone is insufficient to meet the high-end market demands of today. Fitting all the essential components into a single plane gets harder as VLSI circuits get denser and more complicated. Longer interconnects, more power consumption, and slower communication between various circuit components are the results of this.

3D INTEGRATION

3D integration solves these constraints by vertically stacking many layers of transistors and interconnects, enabling for more transistors to be placed in a smaller area. This results in a higher level of integration, faster communication between circuit components, and improved power efficiency. Furthermore, 3D integration enables heterogeneous integration, which allows for the combination of different types of chips, such as memory and processing chips, in a single package. As a result, designs become more efficient and cost-effective, as well as perform better. There are several techniques used for 3D integration, including through-silicon vias (TSVs), which are vertical interconnects that pass through the silicon substrate, and wafer bonding, which involves bonding two or more wafers together to create a single integrated structure. Other techniques include flip-chip bonding, which involves placing the active side of a chip face-down on the substrate and die stacking, which involves stacking chips on top of one another.

Through-silicon vias (TSVs)

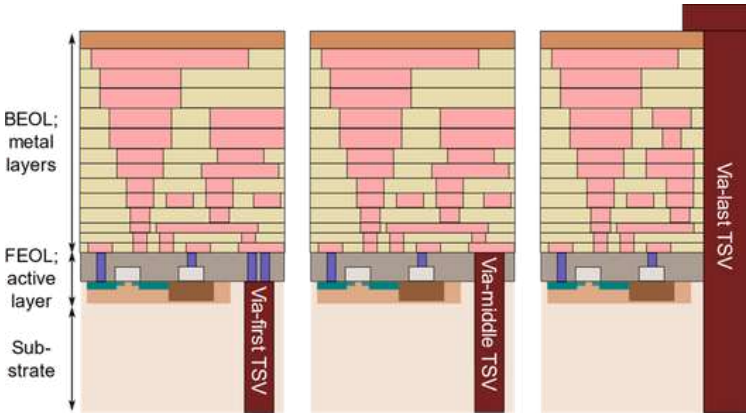
TSVs are vertical electrical interconnects that flow through the silicon substrate of a semiconductor device or chip, linking the device's front-end and back-end layers. TSVs provide communication between vertically stacked layers of transistors and interconnects in 3D integration technology.

TSVs are divided into three categories: Via-first TSVs are created prior to the patterning

of the individual components (such as transistors, capacitors, and resistors), via-middle TSVs are created following the patterning of the individual components but before the metal layers, and via-last TSVs are created following (or during) the BEOL process. TSVs with via-middle connections are currently a common choice for advanced 3D ICs and interposer stacks.

TSVs are often created by etching a hole through a silicon substrate and filling it with copper, tungsten, or aluminium, or another conductive material. This creates a vertical connector that can be utilized to transfer electrical signals between the 3D integrated device's layers. They outperform traditional interconnects such as wire bonding and flip-chip bonding in various ways. TSVs can drastically reduce interconnect lengths, resulting in speedier communication between different components of the device. Furthermore, because they allow for more efficient power delivery and heat dissipation, TSVs can help to reduce power consumption and improve thermal management.

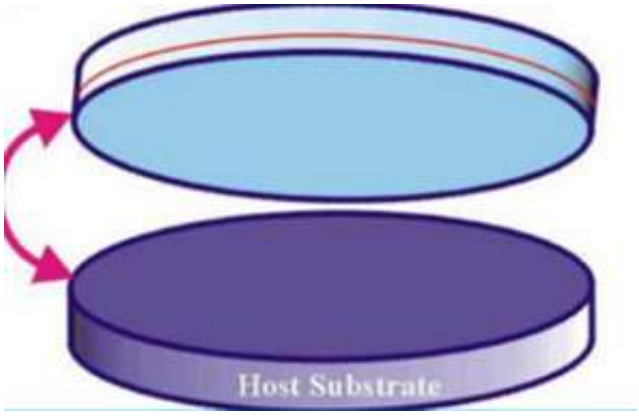
While TSVs have many advantages, they also have some drawbacks, such as the need for precise alignment and bonding between different layers, as well as stress and reliability issues. However, it is expected that with continued advancements in TSV technology and manufacturing processes, these challenges will be overcome, and TSVs will continue to play an important role in the development of advanced 3D integrated circuits.



Wafer bonding

The technique of attaching two semiconductor wafers or substrates together to form a single structure is known as wafer bonding. The procedure calls for the application of pressure and heat, as well as, occasionally, the use of adhesives or other materials for bonding. There are several techniques used in wafer bonding, they are Direct bonding, Anodic bonding, and Adhesive bonding.

Direct bonding: In this process, two flat, pristine wafers are brought together under pressure without the use of a middle layer. Chemical bonds are created at the interface of the two wafers, which links the wafers together.



Direct Wafer bonding

Anodic bonding: With this technique, a strong electric field is applied across the interface between two wafers, one of which is made of a cathodic material (such as silicon) and the other of which is an anodic material (such as glass). The procedure causes the wafers to permanently link together

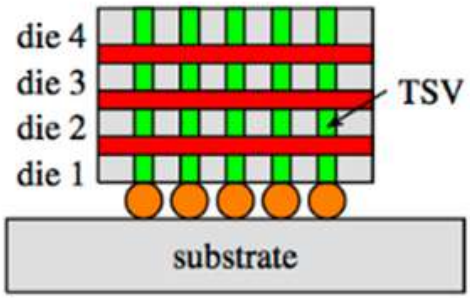
Adhesive bonding: This method entails coating one or both of the wafers with an adhesive or bonding substance prior to bonding. In order to form a solid connection between the wafers, the adhesive is commonly a polymer-based substance that is cured under pressure and heat.

Flip-chip bonding

When a semiconductor device is turned over and electrical connections are formed to the underlying substrate or printed circuit board (PCB), this process is known as "flip chip bonding." In this method, the matching pads on the substrate or PCB are lined up with the active side of the semiconductor device, which is often a chip. Through a series of conductive bumps or solder balls attached to the bonding pads on the device, substrate, and PCB, the electrical connections are made. Flip chip bonding is commonly used in a variety of applications, including microprocessors, memory devices, and image sensors, among others.

Die stacking

Die stacking is a 3D integration technique where multiple semiconductors dies (or chips) are vertically stacked on top of each other and interconnected using through-silicon vias (TSVs) and micro bumps. In this technique, each die is individually processed and then bonded to the next layer using a bonding material, such as adhesive, solder or eutectic material.



Die stacking structure

ADVANCED TECHNOLOGIES IN 3D INTEGRATION

Monolithic 3D integration

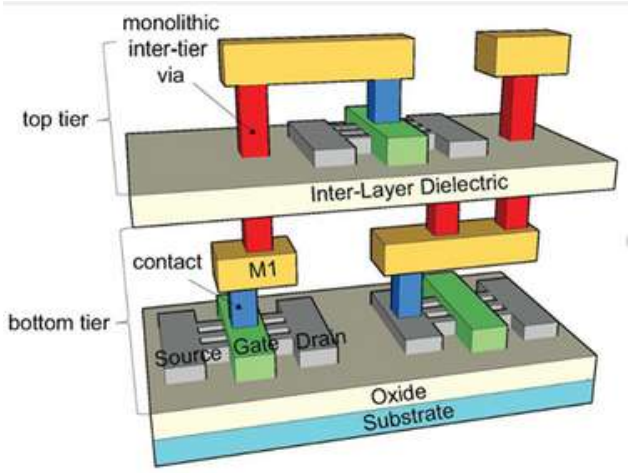
The manufacture of numerous layers of transistors and interconnects on a single silicon wafer is the basis of the cutting-edge 3D integration technique known as monolithic 3D integration. In conventional 2D integration, transistors and interconnects are made on a single silicon layer, with the interconnects connecting the various components along their horizontal axes. As a result, fewer components can be integrated into a single chip at a given density.

Through-silicon vias (TSVs) are used to connect the layers in monolithic 3D integration, which involves stacking numerous layers of transistors and interconnects vertically on a single silicon wafer. Higher performance and less power consumption are produced as a result of the ability to integrate more components into a smaller space. Additionally, the Monolithic 3D chip's shorter interconnects consume less power and have less signal delay than longer interconnects found in conventional 2D integration.

Sequential and concurrent integration are the two primary methods of monolithic 3D integration. Sequential Monolithic 3D integration involves fabricating the layers one at a time, processing each layer before bonding it to the one before it.

Multiple layers are processed concurrently in concurrent monolithic 3D integration, and the TSVs are created during the fabrication process.

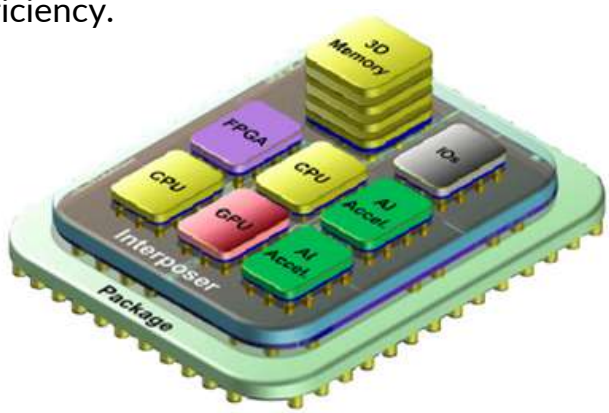
Monolithic 3D integration, which enables the development of highly integrated and high-performance systems in a tiny form factor, is a promising technique for the future of VLSI circuits. But to put it into practice, it requires significant improvements in the fields of materials science, process technology, and design tools.



Structure of monolithic 3D IC based on FinFET technology.

Chiplets

Chiplets are small, pre-validated components that can be combined to form larger systems. Instead of integrating all of the components of a system onto a single chip, chiplets allow for the integration of different functions and components onto separate chips, which can then be combined to form a larger system. Chiplets are a promising technology for the future of VLSI circuits, enabling the creation of highly integrated systems with greater flexibility, reusability, scalability, and cost efficiency.



Chiplet partitioning concept

Hybrid bonding

Hybrid bonding is a technique for forming robust, long-lasting connections between many chip layers or distinct chips. In hybrid bonding, the layers or chips are connected by combining physical and chemical bonding mechanisms, creating a connection that is very solid and dependable.

Different chip types, such as logic and memory chips, can be combined into a single package using hybrid bonding. This makes it possible to build highly integrated systems with enhanced functionality, lower power requirements, and more compact forms. By joining numerous layers of one chip or several chips together, hybrid bonding can also be utilized to create 3D-integrated structures.

Hybrid bonds can be created via a variety of techniques, such as metal-to-metal, polymer, and oxide-to-oxide bonding. Metal-to-metal bonding entails employing a metallic bond to bind two metal surfaces together, as opposed to connecting two oxide surfaces together. A polymer layer is used in polymer bonding to affix two surfaces.

A promising technology for the next generation of VLSI circuits is hybrid bonding, which paves the way for the development of highly integrated, high-performance systems with enhanced reliability and manufacturability. But to put it into practice, it requires significant improvements in the fields of materials science, process technology, and design tools.

Implementation of 3D Integration in VLSI Circuits

There are various phases involved in implementing 3D integration in VLSI circuits. First, computer-aided design (CAD) tools are used to create the circuit's various layers. The layers are then individually constructed using conventional VLSI production methods. After the layers are created, one of the aforementioned 3D integration methods is used to bond them together.

The right alignment of the various layers is one of the main difficulties in establishing 3D integration. This necessitates meticulous manufacture, design, and bonding methods. Managing the heat produced by the circuit is another difficulty because adding layers might raise temperatures. To guarantee that the circuit operates at safe operating temperatures, thorough thermal planning is necessary.

Benefits of 3D Integration

Integration of 3D technology has several advantages. The capacity to enhance circuit density, which can result in smaller and more potent devices, is one of the biggest benefits. This is crucial in applications with constrained space, including wearable technologies and mobile devices. Additionally, 3D integration has the potential to increase power efficiency and communication between various components of the circuit.

Heterogeneous integration, which entails mixing various chip types, such as memory and processor chips, in a single package, is another advantage of 3D integration. This may result in designs that perform better and are more cost-effective.

Conclusion

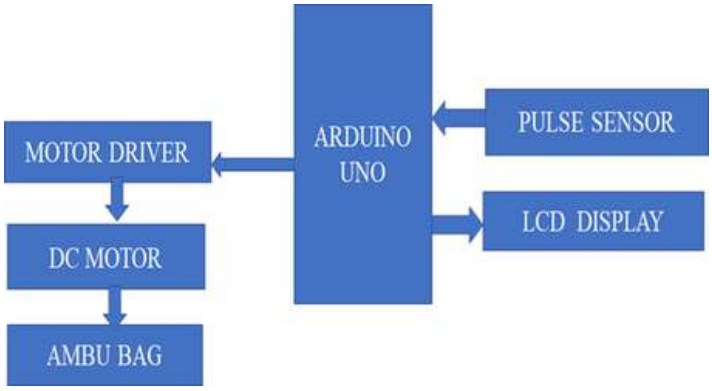
VLSI circuit design and implementation now heavily rely on the 3D integration technology. Numerous advantages are provided, such as increased circuit density, quicker communication, and enhanced power effectiveness. To ensure that the various layers are perfectly aligned, 3D integration implementation calls for meticulous design and fabrication as well as accurate bonding processes. Future VLSI circuits should be considerably more potent and effective thanks to ongoing developments in 3D integration.

STUDENT ARTICLE

AUTOMATED AMBU-BAG

S. HARIPRIYA, IV Year ECE

A person with insufficient breathing is provided with appropriate ventilation using an AMBU bag, a self-inflating bag. The ventilation equipment that is now in use is highly expensive and operates efficiently only with experienced personnel. Ventilators are typically scarce and only found in multispecialty hospitals in underdeveloped nations. We have therefore developed a device that is a low-cost, quickly assemblable, portable, automated AMBU resuscitator system that is easily scaleable in order to address the urgent need for ventilators. By selecting different control modes according to age, it has a significant advantage to use a multi-functional AMBU bag to give essential air to all elderly people with breathing issues. Thus, in the event of an emergency, this device serves as medical assistance.

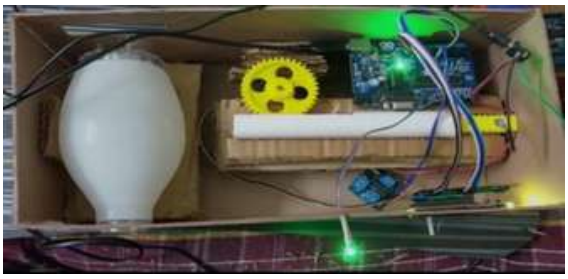


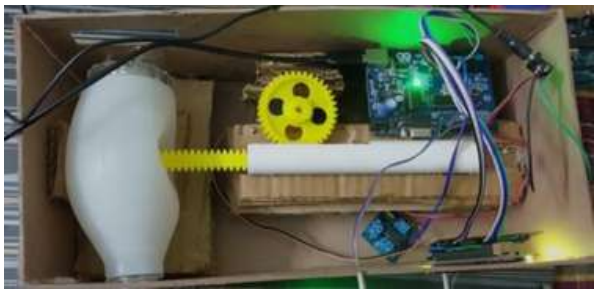
The pulse sensor, which reads the rate of human blood pressure (BP) and displays the rate on an LCD, is used to carry out the process. The principle on which the pulse sensor works is that it must be placed on the veins of a human body, and the light emitted by the LED falls on the veins. The flow of blood inside the vein is done by the pumping of the heart. Measuring the flow of blood is used to calculate the blood pressure. This information is fed to the Arduino. An electronic component known as a motor driver serves as the link between the Arduino and the motors. According to the rate shown on the LCD, the DC motor rotates at a certain speed. The mechanical arm-like structure is moved by the motor and the gear that is attached to it. In order to apply the best pressure to the bag valve, the mechanical arm is rotated forward and back at a specific pace. By compressing the bag, air is pumped into the patient's lungs while the mask is positioned over the patient's airway. The bag then refills itself with air when released, allowing it to return to its original shape.

Measuring Pulse rate using the pulse sensor

Displaying the Pulse rate in LCD

The automated AMBU bag resuscitator may offer an affordable solution to the lack of ventilators. Clinical trials of the automated AMBU bag are necessary to establish safety and efficacy before use in patients with diverse aetiologies of respiratory failure. The device resolves the issue of prolonged manual pressing operations being required and aids in remote monitoring and control to assist effective labour management. In conclusion, this device overcomes all the challenges, making it ideal to help the medical professional by minimising interaction with the patient. It also serves as a last option in the event that a critical care mechanical ventilator is not available.





Compressing the AMBU bag by linear roboticarm

EVENTS CONDUCTED

- IETE-SF and FODSE organized a 24 Hours Intercollegiate Hackathon “Ease The Error 3.0” from 15th May 2023 to 16th May 2023 for 86 intercollegiate students. Dr. K.S. Badrinathan Dean (Educational Development), SVCE. Mr.Maurya Vijayaramachandran, ECE Alumni 2017-21. Mr.Shravan Srivatsan, INT Alumni 2017-21 was the invited dignitaries.

- Dr.R.Gayathri and team Organized a National conference on Signal Processing communication and Networking (NCSPCN -2023)on May 9th 2023.

- ECEA, IETE & RAIC of SVCE organized the Valedictory Function of ECEA, IETE-SF & RAIC for the year 2022-23 on 16/05/2023. Mr. C V Gowri Sankar, Former National Secretary of NIQR was invited as chief guest and he delivered a talk on “Awareness Program on Industry 4.0” It was organized under offline mode for 100 ECE Students.

ACHIEVEMENTS

BY FACULTY

- Dr.T.J.Jeyaprabha, ASP, ECE, Mr.P.Muthukumaran, AP, ECE, Mr.P.Arul, AP, ECE and Mr.L.K.Balaji Vignesh, AP, ECE acted as Juries in the 24 hours inter-collegiate Hackathon Ease the Error 3.0 organized by the Department of ECE and Information Technology, SVCE in association with Forum of Data Science Engineers and IETE Chennai Centre from 15.05.2023 to 16.05.2023.

- Dr.G.A.Sathish Kumar, Dr.R.Gayathri, and Dr.A.Prasanth received a certificate of appreciation for higher H index from the Director (Research), Anna University on 26/5/2023.

- Dr.T.J.Jeyaprabha received 20 Years Long Service Award from SVCE Management on College Day, 5th May 2023

BY UG STUDENTS

- Third-year ECE students Pooja V, Nivetha P, and Ashwini of the Biotech department mentored by S.M.Mehzabeen secured First position with a cash award of Rs2000/- in the National Conference on Signal Processing Communication and Networking (NCSPCN -2023) paper titled “3D CNN Based Approach for Identification of Schizophrenia using functional MRI” conducted by Department of ECE on May 9th, 2023.

- Final year students SANGEETH KANNA P, SRIVANTH A, VINSON XAVIER Y mentored by Mrs.S.M.ABINAYA secured SECOND position in National Conference on Signal Processing communication and Networking (NCSPCN -2023) paper titled “SMART SHOPPING TROLLEY FOR VISUALLY IMPAIRED PEOPLE” conducted by Department of ECE on May 9th 2023.

- Krishnavignesh R, Mohamed Afsar M, Snehayaazhini S mentored by Dr. T.J. Jeyaprabha received Best Paper Award in National Conference on Signal Processing communication and Networking (NCSPCN -2023) paper titled “1-WIRED UART-BASED COMMUNICATION MANAGEMENT SYSTEM" conducted by the Department of ECE on May 9th 2023.

- Ms.SAHANA BALASUBRAMANIAM, Mr. RASWANTH U, Ms. AISWARYA SRINIVASAN, Mr. RAJA PANDI (Team ID-1681) mentored by Dr T J Jeyaprabha won the prelims of Innovation Challenge 2023 event organized by IEEE in Panimalar Institute of Technology. The team is shortlisted for finals in Egypt.

- VISHNU PRIYA V T, R. Supraja, Rajeshvar M Swamy, Sudarshan C mentored by Dr T J Jeyaprabha won the prelims of the Innovation Challenge 2023 event organized by IEEE in Panimalar Institute of Technology. The team is shortlisted for finals in Egypt.

- Ms.B.Elakkiya participated in 5 days TiHAAN Sponsored workshop on “Drone Based Aerial Survey and Image Processing” conducted by Vellore Institute of Technology Chennai from 29.05.2023 to 02.06.2023.

- Siddique Afraaz N, Ugendran R Yukesh Kumar S, Dr.T.J.Jeyaprabha participated and presented their manuscript titled “A COMPREHENSIVE ANALYSIS OF ADVANCED THREAT PROTECTION TECHNOLOGIES IN MODERN ENDPOINT MANAGEMENT SYSTEMS” at the National Conference on Signal Processing, Communication and Networking organized by the Department of ECE, SVCE on 9th May 2023.

FACULTY PUBLICATION

- Dr.A.Prasanth published a paper titled “ALBAE feature extraction based lung pneumonia and cancer classification”, Soft Computing, (2023) 1-12.

- S.M.Mehzabeen Pooja V, Nivetha P and Ashwini Published a paper titled “3D CNN Based approach for Identification of Schizophrenia using functional MRI “in the Proceedings of National Conference on Signal Processing communication and Networking (NCSPCN -2023)conducted by Department of ECE on May 9th 2023.

- S.M.Mehzabeen,Anu shobika ,Diya Rajiv Christopher and Afrin KhanPublished a paper titled”Design of CNN based Classifier for identification of rice plant disease”in the Proceedings of National Conference on Signal Processing communication and Networking (NCSPCN -2023)conducted by Department of ECE on May 9th 2023.

- S.Nandhini,Dr.R.Gayathri,S.M.Mehzabeen Published a paper titled”LIVER ULTRASOUND IMAGE ENHANCEMENT AND ABNORMALITY CLASSIFICATION IN MACHINE LEARNING”in the Proceedings of National Conference on Signal Processing communication and Networking (NCSPCN -2023)conducted by the Department of ECE on May 9th 2023.

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REVIEWER/EDITORIAL BOARD MEMBERS

- G.A.Sathish Kumar reviewed a Book Chapter entitled “Mining Frequent Itemsets with Fuzzy Taxonomic Structures for Cybercrime Investigations”, B P International, India, May 2023.

- Mr. N. Sathish reviewed three papers in the 2023 International Conference on Signal Processing, Computation, Electronics, Power and Telecommunication (IConSCEPT)”, organized by the Departments of ECE, EEE, and CSE at the National Institute of Technology Puducherry on 25th and 26th May 2023.

- Mr.L.K.Balaji Vignesh reviewed Six Papers in AICTE Sponsored “IEEE International Conference on Networks, Multimedia and Information Technology (NMITCON)” organized by the Department of Electronics and Communication Engineering, Nitte Meenakshi Institute of Technology, Bengaluru.

- Dr.T.J.Jeyaprabha reviewed papers for AICTE Sponsored “IEEE International Conference on Networks, Multimedia and Information Technology (NMITCON)” organized by the Department of Electronics and Communication Engineering, Nitte Meenakshi Institute of Technology, Bengaluru.

INTERNSHIP

- Third year students Kabilan S,Manishkumar M, Naveenkumar S, Mohamed Fisal T and Mervin Jerel D underwent Internship at NSIC Technical Services Centre, Chennai, for a period of 15 days from 24/04/2023 to 08/05/2023

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- Sri Rekha T of third year underwent Internship at Wiztech Automation Solutions Pvt. Ltd., Chennai, for a period of 14 days from 01/05/2023 to 14/05/2023

INDUSTRIAL VISIT

- First-year ECE Students have undergone Industrial visits to Retech Lasers, Tambaram, Chennai from 15.05.2023, 17.05.2023 and 18.05.2023

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STUDENT EDITORS

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