BIPOLAR JUNCTION TRANSISTOR

Introduction:

Transistor:

A bipolar junction transistor (BJT) has two PN-junctions. It is a device which transforms current flow from a low resistance path to a high resistance path. This transfer of current through resistance has given the name to the device transfer resistor or transistor. Since this device is made up of two junction diodes. It is generally called junction transistor.

There are two types of junction transistors:

Uni-polar junction transistors	Bipolar junction transistors
Only majority carrier's transport the current.	Interaction of both the majority and minority carriers transport the current.

Constructional Details:

A bipolar junction transistor is simply a sandwich of one type of semiconductor material (p-type or n-type) between two layers of the other type. A block representation of a layer of n-type material between two layers of p-type is shown in Figure: (a). This is described as PNP transistor. Figure: (b). shows an NPN transistor, consisting of a layer of p-type material between two layers of n-type.

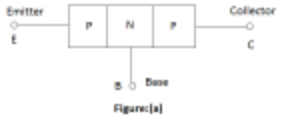


Figure:(a)

Figure:(c)

Figure:(b)

Figure:(d)

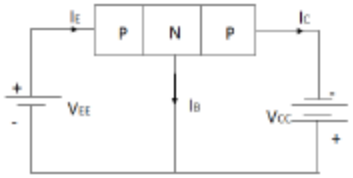
The center layer is called the base, one of the outer layers is termed the emitter, and the other outer layer is referred to as the collector. The emitter, base and collector are provided with terminals, which are appropriately labeled E, B, and C. Two PN junctions exist within each transistor: the collector-base junction and the emitter-base junction.

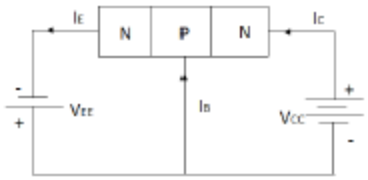
Circuit symbols for PNP and NPN transistors Figure: (c) and Figure: (d) together with the corresponding block representations. The arrowhead on each symbol always identifies the emitter terminal of the transistor. Also, in each case its direction indicates the conventional direction of current flow. For the NPN transistor, the arrowhead points from the p-type base to the n-type emitter. For the PNP transistor, it points from the p-type base. Thus, the arrowhead is always from p to n.

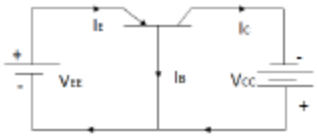
The center layer of the transistor is made very much narrower than the two outer layers. Also the outer layers are much more heavily doped than the center layer. This causes the depletions regions to penetrate deeply into the base, and thus the distance between the emitter-base (EB) and collector-base (CB) depletion regions is minimized.

Transistor Biasing:

The application of a suitable D.C. voltage, across the transistor terminals is called Biasing.







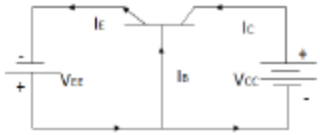


Figure (a) : PNP transistor **Figure (b) : NPN transistor**

In order to have a normal function of transistor it is necessary to apply voltage of a correct polarity across its two junctions. This is called biasing. The bias and supply voltage polarities for NPN and PNP transistors are shown in fig (a) & (b). For NPN points from the (positive) base to the (negative) emitter. The collector is then biased to a higher positive level than the base. For a PNP device the base is negative with respect to the emitter. The arrowhead a point from the (positive) emitter to the (negative) base, and the collector is then more negative than the base. Typical base-emitter voltages for both NPN and PNP transistors are 0.7V for silicon and 0.3V for germanium.

TRANSISTOR OPERATION:

PNP Transistor:

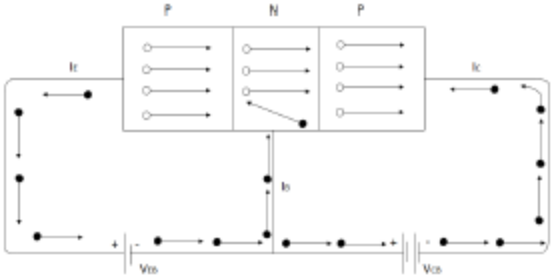


Fig shows the basic connection of a PNP transistor. A small value battery B_1 forward biases the emitter-base junction of a PNP and the collector-base junction is reverse biased by a high value battery B_2. The positive terminal of the battery B_1 repels the holes in the P-region on the left. These holes in the P-Type emitter to flow towards the base. This constitutes the emitter current I_E. As these holes cross into the N-Type base, they tend to combine with the electrons. As the base is lightly doped and very thin, therefore only a few holes (less than 5%) combine with the electrons. The remainders (more than 95%)

cross into the collector region. The negative terminal of the battery B_2 attracts these holes. This constitutes the collector current I_c. In this way almost the entire emitter current flows in the collector circuit. It may be noted that current conduction with in PNP transistor is by holes. Therefore, the emitter current

$$I_E = I_B + I_C.$$

NPN Transistor:

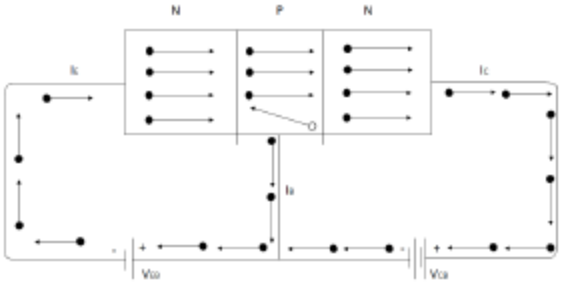


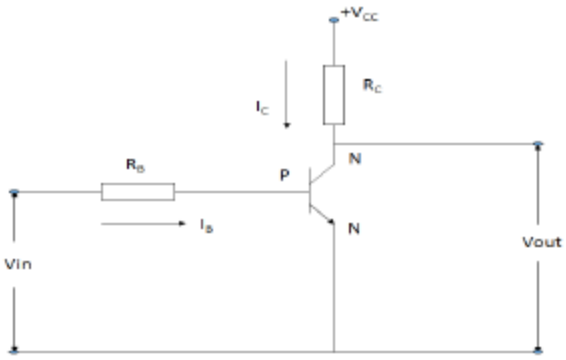
Fig shows the basic connection of a NPN Transistor. A small value battery B_1 forward biases the emitter-base junction of a NPN and the collector–base junction is reverse biased by a high value battery B_2. The negative terminal of the battery B_1 repels the electrons in the N-region on the left. This electron in the N-Type emitter to flow towards the base. This constitutes the emitter current I_E. As these electrons cross into the P-Type base, they tend to combine with the holes. As the base is lightly doped and very thin, therefore only a few electrons (less than 5%) combine with the holes. The remainder (more than 95%) crosses into the collector region. The positive terminal of the battery B_2 attracts these electrons. This constitutes the collector current I_C. In this way almost the entire emitter current flows in the collector circuit. It may be noted that current conduction with in NPN transistor is by electrons. Therefore, the emitter current

$$I_E = I_B + I_C.$$

Transistor as a switch:

The transistor as a switch operates between two states namely saturation and cut off state. The typical transistor circuit is shown in figure. It consists of a transistor with collector load resistance R_c. The input is given at base terminal and output is taken at collector terminal.

When the input signal is negative, the emitter base junction will reverse biased and the transistor never comes to conduction state. The transistor will be in cut off and no current flows in the load resistance R_c. As a result, there is no voltage drop across R_c.



Hence the output voltage will be supply voltage i.e.V_o= V_{cc}. It is equal to open circuit voltage since the transistor is in cut off.

When the input voltage is positive, it forward biases the base-emitter junction and the transistor will come to conduction state. Now maximum current will be flowing from collector to emitter and all the V_{cc} is dropped across R_c. Thus the output voltage will be zero. i.e. V_o=0. Hence the transistor is turned on and off depending upon whether the input bias voltage is positive or negative. Thus a transistor can act as a switch.

Advantages:

1. It has no moving point.
2. It gives noiseless operation.
3. It has smaller size and weight.
4. It gives trouble free service because of solid state.
5. It is cheaper than other switches.
6. It requires less maintenance.
7. It has a very fast speed of switching operation.

TRANSISTOR AS AN AMPLIFIER:

The operation of a transistor as an amplifier is based on the fact that base current, I_B in a transistor can control the collector current, I_C. The base current can be varied by variation of forward bias and this produce corresponding variation in the collector current.

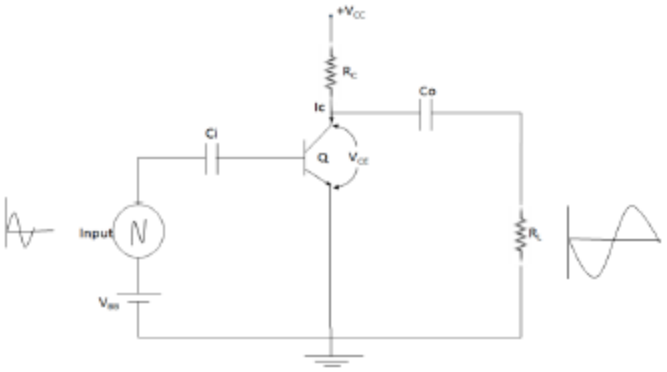


Figure : Transistor as an amplifier

The weak signal is applied between emitter-base junction and output is taken across the load R_c connected in the collector circuit. The emitter-base junction in a transistor is forward-biased and, as such the input impedance is low. On the other hand, the base-collector is reverse biased and hence the output impedance is very high. A D.C voltage V_{EE} is applied in the input circuit in addition to the signal. This D.C voltage magnitude is such that it always keeps the input forward biased regardless of the polarity of the signal.

Even a small change in signal voltage caused an appreciable change in emitter current, since the input circuit has low resistance. Due to transistor action the same change in collector current take place. The collector flows through a large load resistance (Rc), which in turn produces a large voltage across it. Thus a weak signal applied in the input circuit appears in the amplified form in the collector circuit. In this way transistor acts as an amplifier.

TRANSISTOR BIASING:

The amplifiers which are used to magnify the weak signal without change in its wave shape and frequency are called faithful amplifiers. For faithful amplifications, the transistor amplifier must satisfy three basic conditions. They are namely:

1. Proper zero signal collector current.
2. Proper base to emitter voltage at any instant.
3. Proper collector to emitter voltage at any instant.

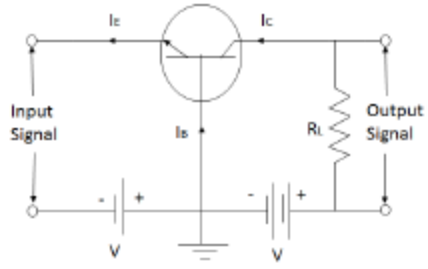
The technique of transistor biasing is used to fulfill the above said three conditions.The Proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as transistor biasing.

The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-emitter junction properly reverse biased during the application of signals. That means the transistor must operate only in active region. This can be achieved by using bias battery of resistor circuit with the transistor. The resistor method is more efficient and is frequently used. The circuit used for proper biasing of the transistor is called biasing circuit. This circuit used to fix the operating point at a particular level for satisfying the above said basic conditions.

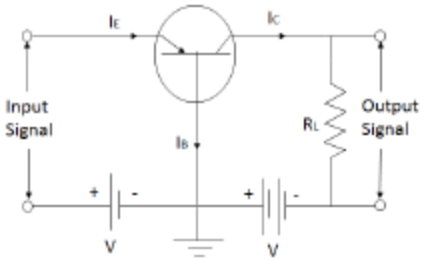
COMMON BASE CHARACTERISTICS:

Common base connection:

In this configuration the input is applied between the emitter and base and the output is taken from the collector and the base. Here the base is common to both the input and the output circuits as shown in fig.



NPN transistor



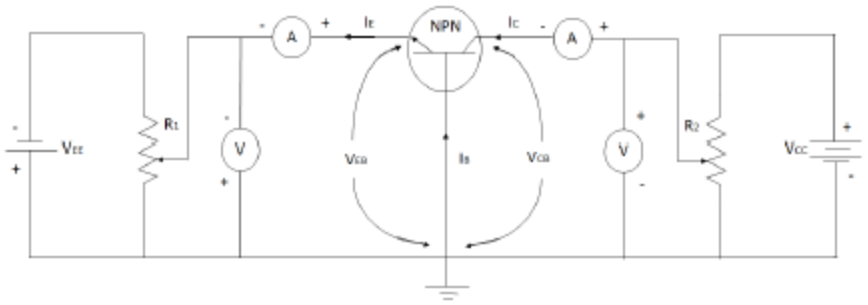
PNP transistor

In a common base configuration, the input current is the emitter current I_E and the collector current I_C. The ratio of change in collector current to the change in emitter current at constant collector-base voltage is called current amplification factor.

$$= \frac{\Delta I_C}{\Delta I_E} \text{ at constant } V_{BC}$$

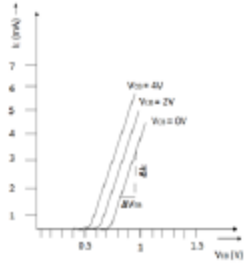
In a transistor V_{EB}, I_E,I_C,V_{CB} are parameters. In the above connection voltmeters and ammeters are connected to measure input and output voltages and currents as shown in fig.

Characteristics of Common Base Configuration:



The circuit arrangement for determining the characteristics of a common base NPN transistor is shown in fig. In this circuit, the collector to base voltage (V_{CB}) can be varied by adjusting the potentiometer R_2. The emitter to base voltage (V_{BE}) can be varied by adjusting the potentiometer R_1. The DC voltmeters and DC millimeters are connected in the emitter and collector circuits to measure the voltages and currents.

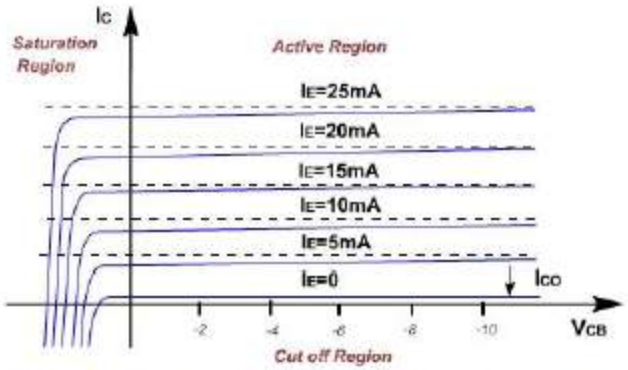
Input characteristics:



The curve plotted between the emitter current (I_E) and the emitter to base voltage (V_{BE}) at constant collector to base voltage (V_{CB}) are known as input characteristics of a transistor in common base configuration.

Output characteristics:

The emitter current I_E is held constant at each of several fixed levels. For each fixed level of I_E, the output voltage V_{CB} is adjusted in convenient steps, and the corresponding levels of collector current I_C are recorded. In this way a table of values is obtained from which a family of output characteristics may be plotted. In fig the corresponding I_C and V_{CB} levels obtained when I_E was held constant at 1mA are plotted, and the resultant characteristic is identified as I_E = 1mA. Similarly, other characteristics are plotted for I_E = 2mA, 3mA, etc.



1. The common base output characteristics in fig. show that for each fixed level of I_E, I_C is almost equal to $I_E$and appears to remain constant when V_{CB} is increased.

2. This characteristic may be used to find the output resistance (r_o).

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

3.A very large change in collector-base voltage produces small change in collector current. It means that the output resistance is very high.

4. The collector is constant above certain values of collector-base voltage. It means that I_C is independent of V_{CB} and depends upon I_E only.

The output characteristics may be divided into three regions and these regions are plotted in the fig.

1. The active region
2. Cut-off region
3. Saturation region

Active region:

In this region the collector junction is reverse biased and the emitter junction is forward biased. In this region when $I_E = 0$, $I_C = I_{CO}$. This reverse saturation current remains constant and is independent of collector voltage V_{CB} as long as V_{CD} is below the breakdown potential.

Saturation region:

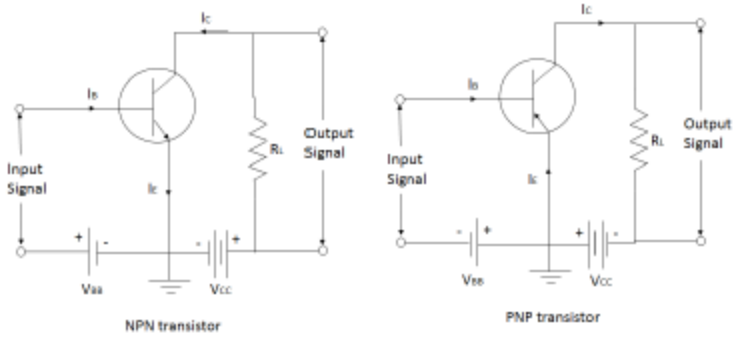
The region to the left of ordinate $V_{CB} = 0$ is called the saturation region. In this region both junction are forward biased.

Cut-off region:

The region below the $I_E = 0$ characteristics, for which the emitter and collector junction both reverse biased is called cut-off region.

COMMON EMITTER CHARACTERISTICS:

Fig. shows the circuit employed for determining transistor common emitter characteristics.

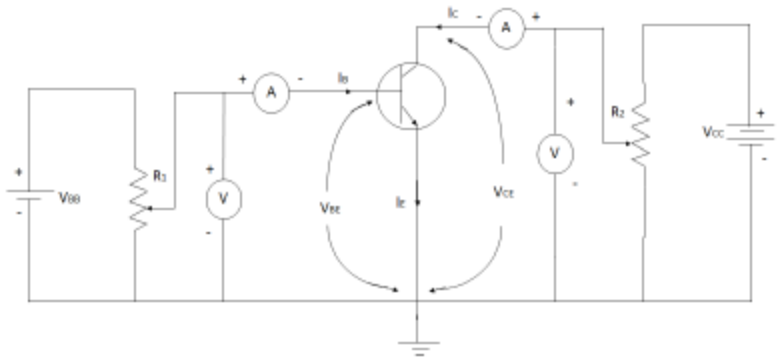


In this configuration, the input is applied between the base and the emitter and the output is taken from the collector and the emitter. In this connection, the common emitter is common to both the input and the output circuits as shown in fig. In the common emitter configuration, the input current is the base current I_B and the output current is the collector current I_C. The ratio of change in collector current to the change in base current at constant collector-emitter voltage is called current amplification factor (β).

$$\beta = \frac{\Delta I_C}{\Delta I_B} \text{ at constant } V_{CE}$$

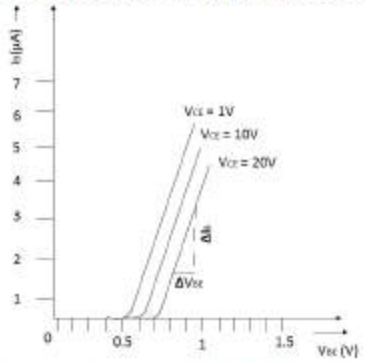
Common Emitter Circuit:

A test circuit for determining the static characteristics of an NPN transistor is shown in fig. In this circuit emitter is common to both input and output circuits. To measure the base and collector current milli ammeters are connected in series with the base and the output circuits. Voltmeters are connected across the input and the output circuits to measure V_{BE} and V_{CE}. There are two potentiometers R_1 and R_2 to vary the supply voltages V_{CC} and V_{BB}.



Input Characteristics:

It is a curve, which shows the relationship between the base current I_B and the emitter-base voltage, V_{BE} at constant V_{CE}. The method of determining the characteristic is as follows.



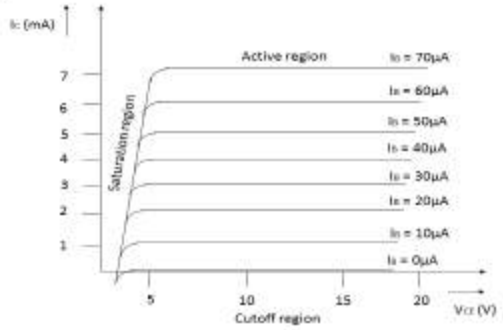
First, by means of R1 suitable voltage is applied from Vcc. Next, voltage V_{BE} is increased in number of steps and corresponding values of I_B are noted. The base shows the input characteristic for common emitter configuration. The following points may be noted from the characteristic.

1. The input resistance of the transistor is equal to the reciprocal of the slope of the input characteristic curve

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B}$$

2. The initial portion of the curve is not linear
3. The input resistance varies considerable from a value of 4-Kilo ohm to a value of 600 ohms
4. In the case of silicon transistor, the curves break away from zero current for voltage in the range of 0.5 to 0.6 volt whereas for germanium transistor the breakaway point in the range 0.1 to 0.2V.

Output Characteristics:



Missing Pulse Detector

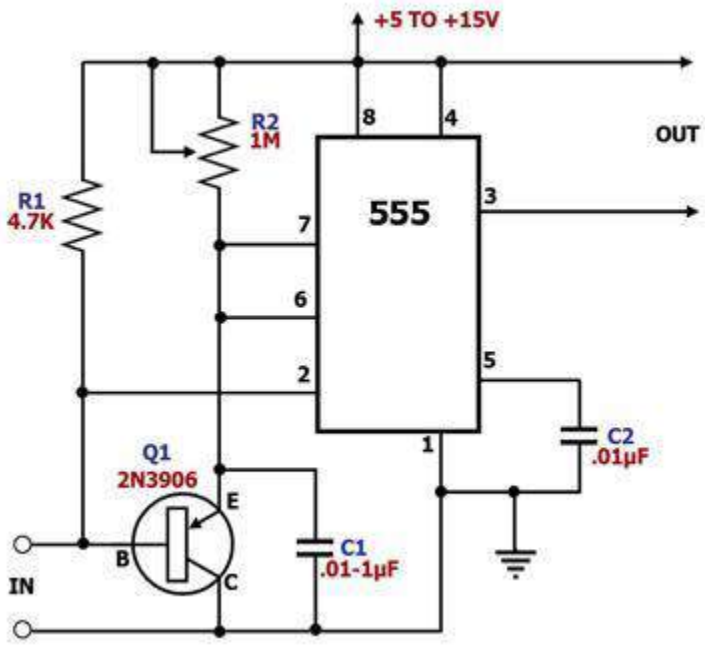


Figure 1. Missing Pulse Detector Circuit Diagram

This circuit is a missing pulse detector, i.e., it can be used to detect missing pulses in an incoming pulse train. The main component of this circuit is the 555 timer IC. In this circuit, it is configured as a monostable multivibrator, i.e., a circuit which will output a single pulse every time it is 'triggered'.

Every time a pulse arrives at pin 2 of the 555 timer in this circuit, the 555 is triggered to output a single pulse at pin 3. The width of this output pulse is defined by the values of R2 and C1. R2 and C1 must be chosen such that the output pulse width is slightly greater than the time between each incoming pulse. If the arrival of the pulses at pin 2 is continuous, the output will never complete a single pulse. This is because the 555 timer will always be retriggered and C1 will always be discharged through Q1 every time a new input pulse arrives. As such, the output of pin 3 will always be 'high'.

However, a missing pulse will allow pin 3 to output a complete pulse. This means that it will change its state from 'high' to 'low' after the set pulse width has been attained. Thus, a change in state of the output of this circuit signifies that it has detected a missing pulse in the pulse train arriving at the input.

UNIT 5: SPECIAL FUNCTION ICs

INTRODUCTION

The 555 timer IC was introduced in the year 1970 by Signetic Corporation and gave the name **SE/NE 555 timer**. It is one of the monolithic timing circuits and important use of this IC is providing accurate and constant delay to the circuit. And the other advantages of this IC are very compact size, more reliable, and low cost also. IC555 are very much used in different fields. Some of the applications are given below.

Applications of IC555 are

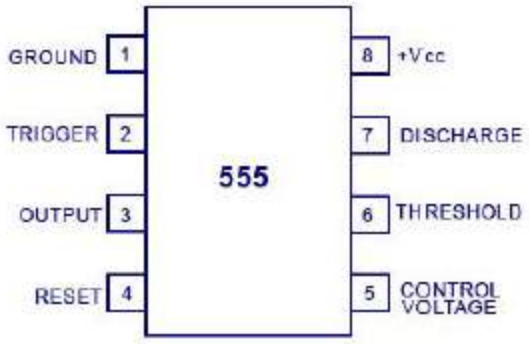
1.Monostable multivibrator

2. Astable multivibrator

3. Wave form generators

4. DC-DC convertor etc.

PIN DIAGRAM OF IC 555



8-Pin DIP

Pin descripion:

Pin 1: Grounded Terminal: The given input voltages and output voltages are measured with respect to ground.

Pin 2: Trigger Terminal: The trigger voltage defines the output of the timer.

Pin 3: Output Terminal: Output of the timer is available at this pin. There are two ways in which a load can be connected to the output terminal. One way is to connect between output pin (pin 3) and ground pin (pin 1) or between pin 3 and supply pin (pin 8). The load connected between output and ground supply pin is called the *normally on load* and that connected between output and ground pin is called the ***normally off load***.

Pin 4: Reset Terminal: It is used to reset the timer .By applying high signal to the terminal it can reset the timer.

Pin 5: Control Voltage Terminal: The amount of control voltage controls the width of the output pulses.

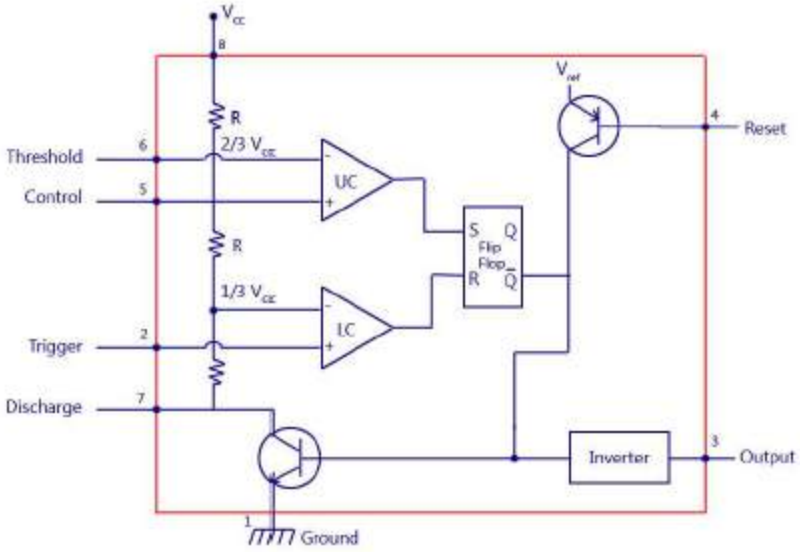
Pin 6: Threshold Terminal: This is the non-inverting input terminal of comparator 1, which compares the voltage applied to the terminal with a reference voltage of 2/3 V_{CC}. If the applied voltage crosses the threshold level then the upper comparator output becomes high and the output goes to low.

Pin 7 : Discharge Terminal: This pin is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal and ground. It is called discharge terminal because when transistor saturates, capacitor discharges through the transistor. When the transistor is cut-off, the capacitor charges at a rate determined by the external resistor and capacitor.

Pin 8: Supply Terminal: the supply voltage range of the IC can be +5v to +18v.

FUNCTIONAL DIAGRAM OF 555 IC

555 IC Timer Block Diagram



WORKING PRINCIPLE

The above block diagram consists of upper and lower comparators , flip flops, invertors ,amplifier and resistive network.

The resistive network connected here are act as a voltage divider which divides the Vcc into 2 levels, one level is 2/3Vcc and one more level is 1/3Vcc. 2/3 Vcc is given to the inverting terminal of upper comparator it is it's threshold level and (1/3)Vcc at the inverting terminal of the lower comparator. The upper and lower comparator are used to set and reset the flip flop and also these 2 comparators are the responsible for charging and discharging the transistor Q1 and Q2 .The upper comparator has the reference level of 2/3 Vcc and the lower comparator has the reference level of 1/3Vcc.In general The threshold voltage and trigger voltage can control the timer , so there is no need of special control voltage given to it. If we

want to change the width of the pulse ,we have to give control voltage separately at pin 5.

When the trigger voltage applied.

When the trigger voltage is applied to the inverting terminal of the comparator C2 through 1/3Vcc at its noninverting terminal, the comparator changes the state of flipflop to set state. Then the output of flip-flop makes the transistor to low level.

When the threshold voltage applied.

When the threshold voltage is applied to the comparator C1 through the reference voltage of 2/3 Vcc, the output of the comparator will also change the state of flipflop to reset. Then the transistor acts as a buffer.

APPLICATIONS OF 555IC

applications as a

1.**Monostable multivibrator**

2. **Astable multivibrator**,

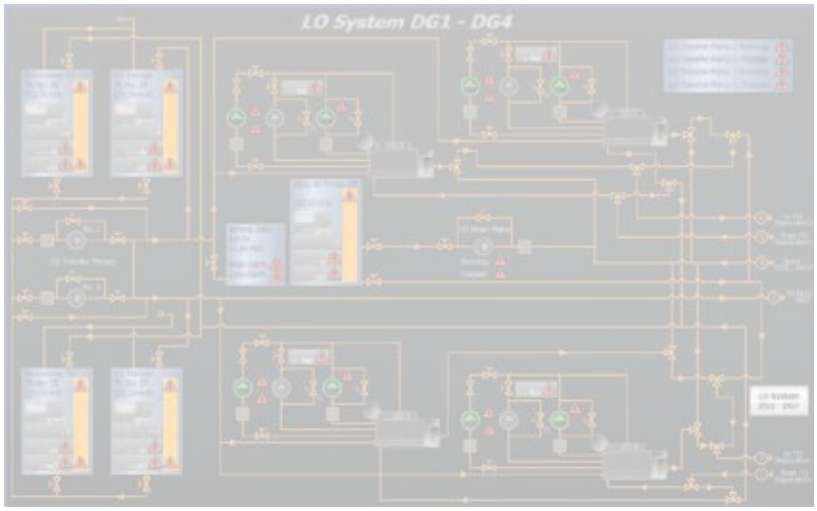
3. Schmitt trigger

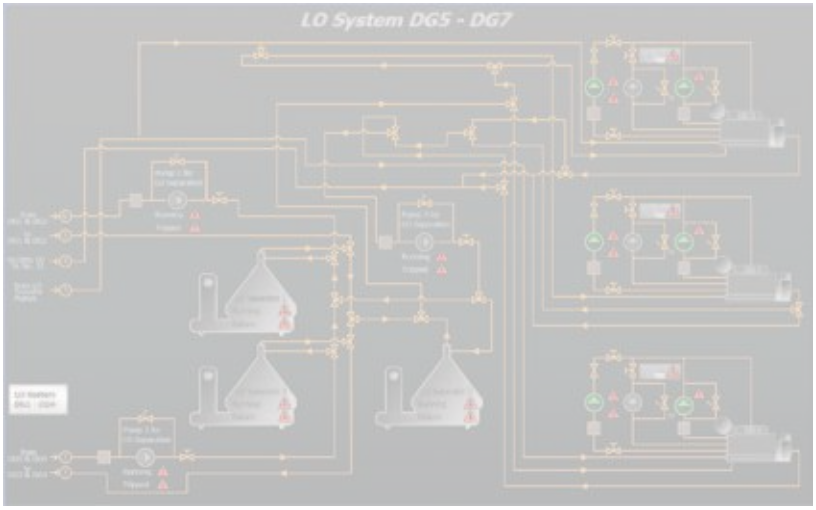
4. **Dc-dc converters**

5. **Waveform generators**

6. **Temperature measurement** and etc.,

Integrated Automation System IAS





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The integrated automation system IAS integrates the functions of control, monitoring and alarming of all automation systems on the ship.

The structure of the system is distributed, it consists of several substations communicated with each other via a redundant, fast and reliable communication protocol. Distributed system structure minimizes cabling to a minimum.

MPL Techma provides the opportunity to develop a system both for newly built vessels as well as a retro-fits of old systems . We also provide service and maintenance of existing systems.

The integrated automation system IAS integrates the functions of the following systems:

1. Engine room alarm and monitoring system
2. Ballast system
3. Tanks sounding system
4. Fuel control system
5. Controlling all valves
6. Electrical energy flow and distribution control
7. Protocol communication with:
    - PMS system
    - VDR system
    - Main engine control systems
    - Auxiliary engines control system
    - Thrusters control system
    - Pumps and fans inverters

Features:

8. Ability to develop a system as a new system or as a retrofit of old system
9. The flexible structure - any configuration adapted to requirements
10. Friendly operator interfaces
11. Fast, redundant and reliable data flow between stations and system interfaces

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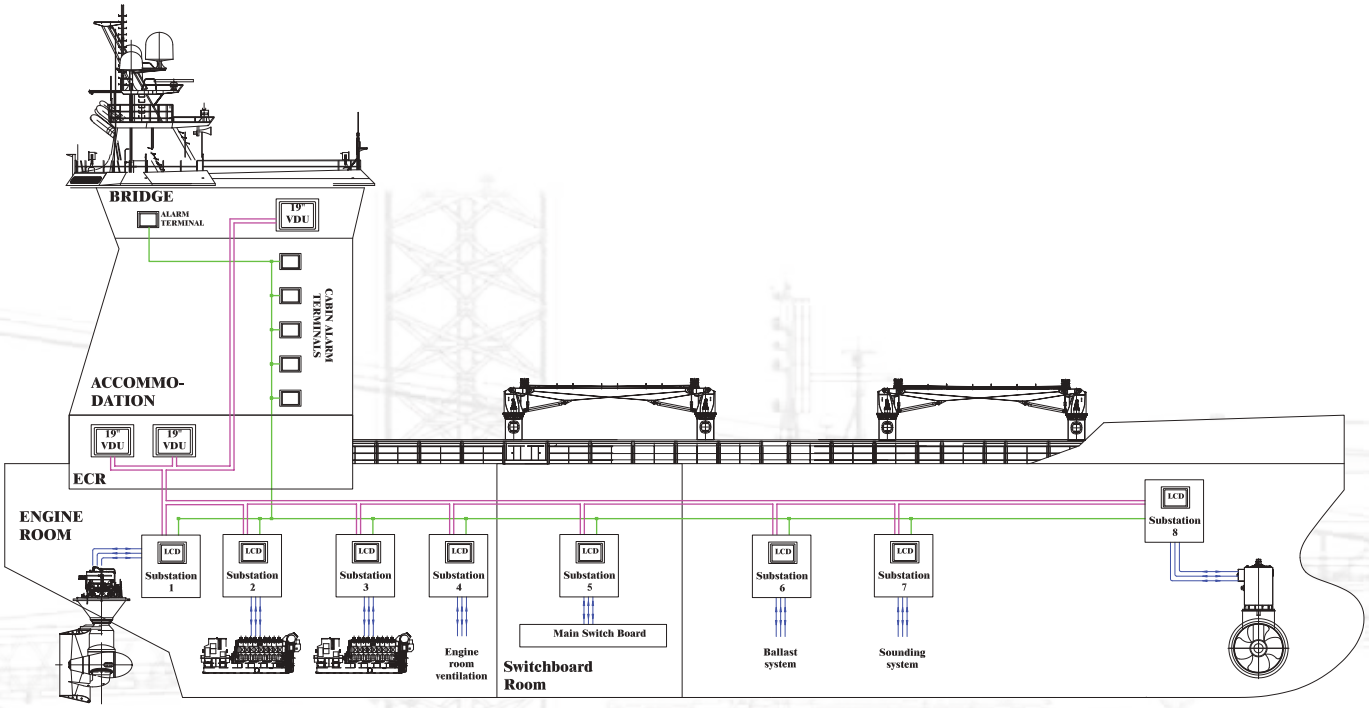

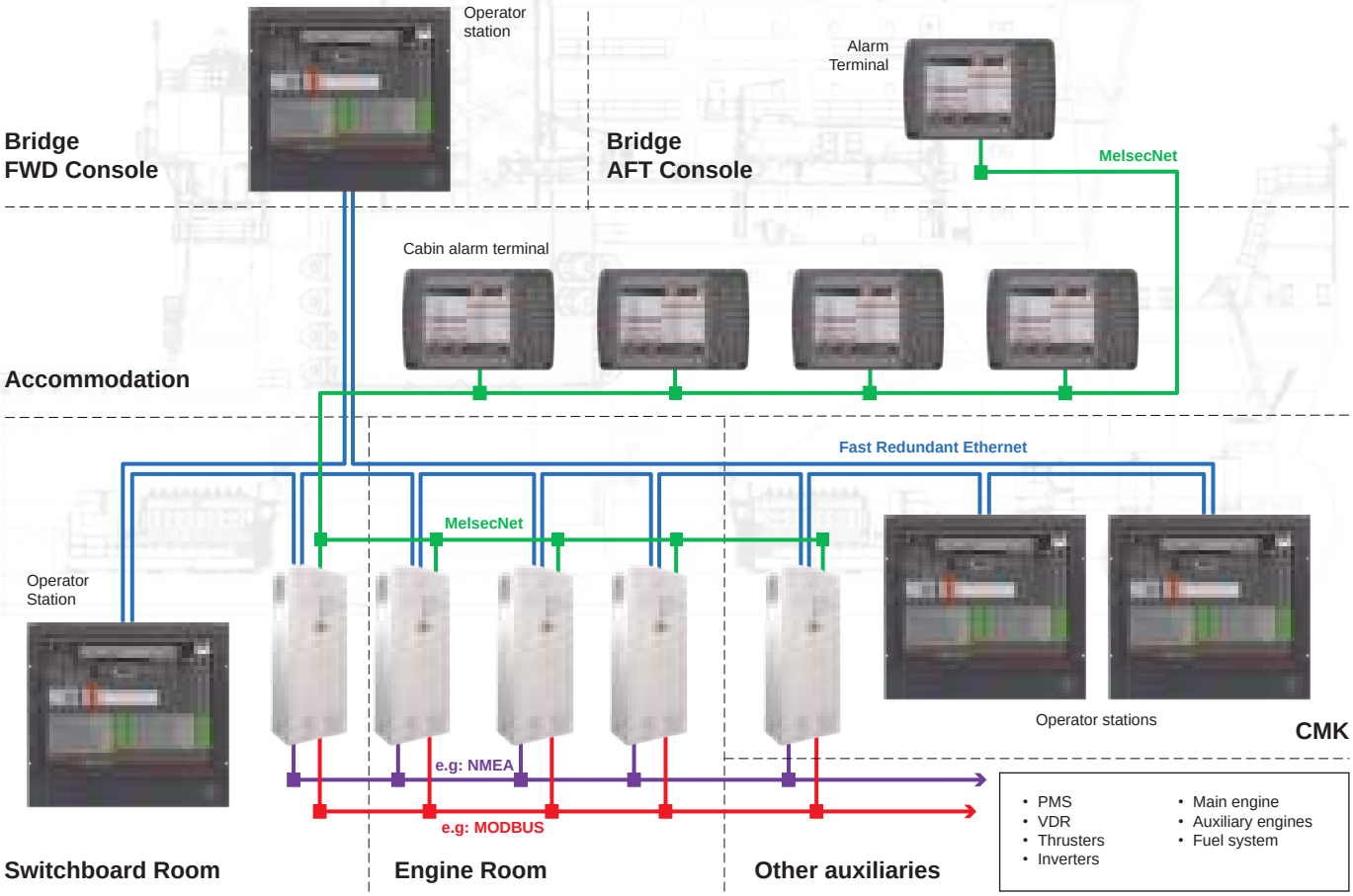

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MPL TECHMA

We cooperate with:

We fulfill the requirements of the leading classification societies:

MPL Techma Ltd
96/98 Al. Zwycięstwa str.
81-451 Gdynia, POLAND
marine@mpltechma.pl
www.mpltechma.pl

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SONAR

KAMAL SINGH

EC111044

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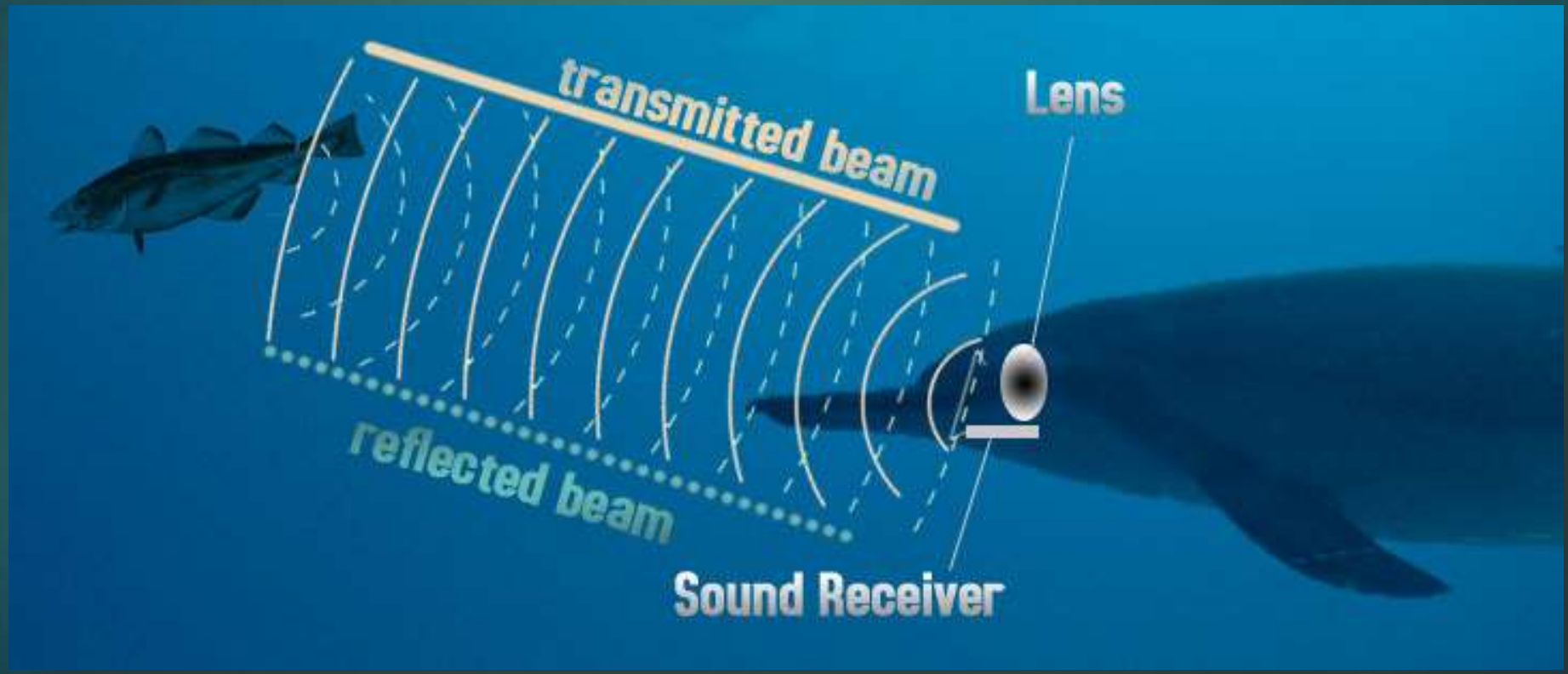
- Introduction
- History of sonar
- Sonar technology
- Active sonar
- Passive sonar
- Performance factor
- Application
- limitation

introduction

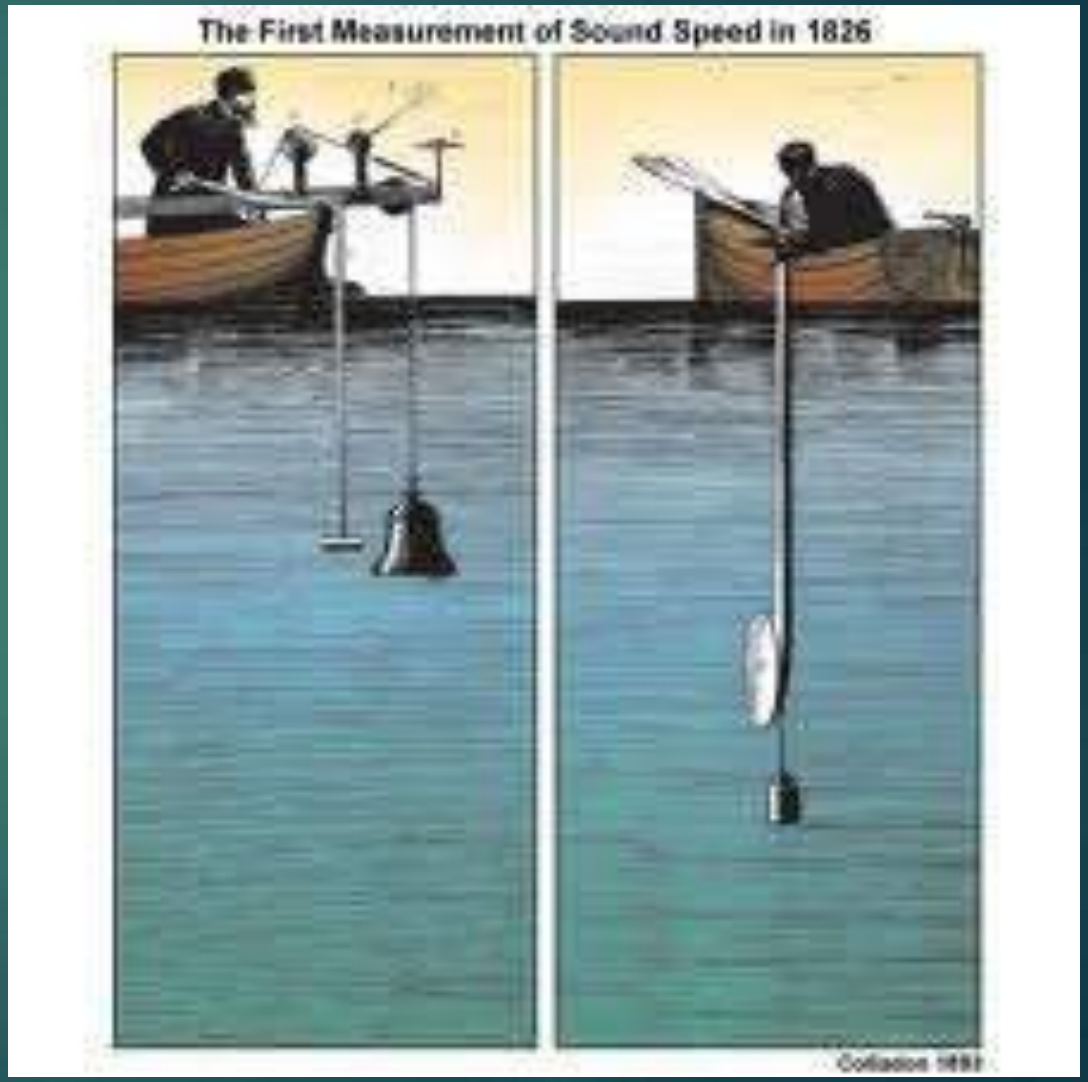
- Sonar ,which in itself originally an acronym for Sound Navigation And Ranging.
- It is a method of detecting , locating ,and determining the speed of objects through the use of reflected sound waves .
- A system using transmitted and reflected underwater sound waves to detect and locate submerged objects
- The acoustic frequencies used in sonar systems vary from very low (infrasonic) to extremely high (ultrasonic).

history

- We know that some animals (dolphins and bats) have use sound as a medium of communication and objects detection for millions of years

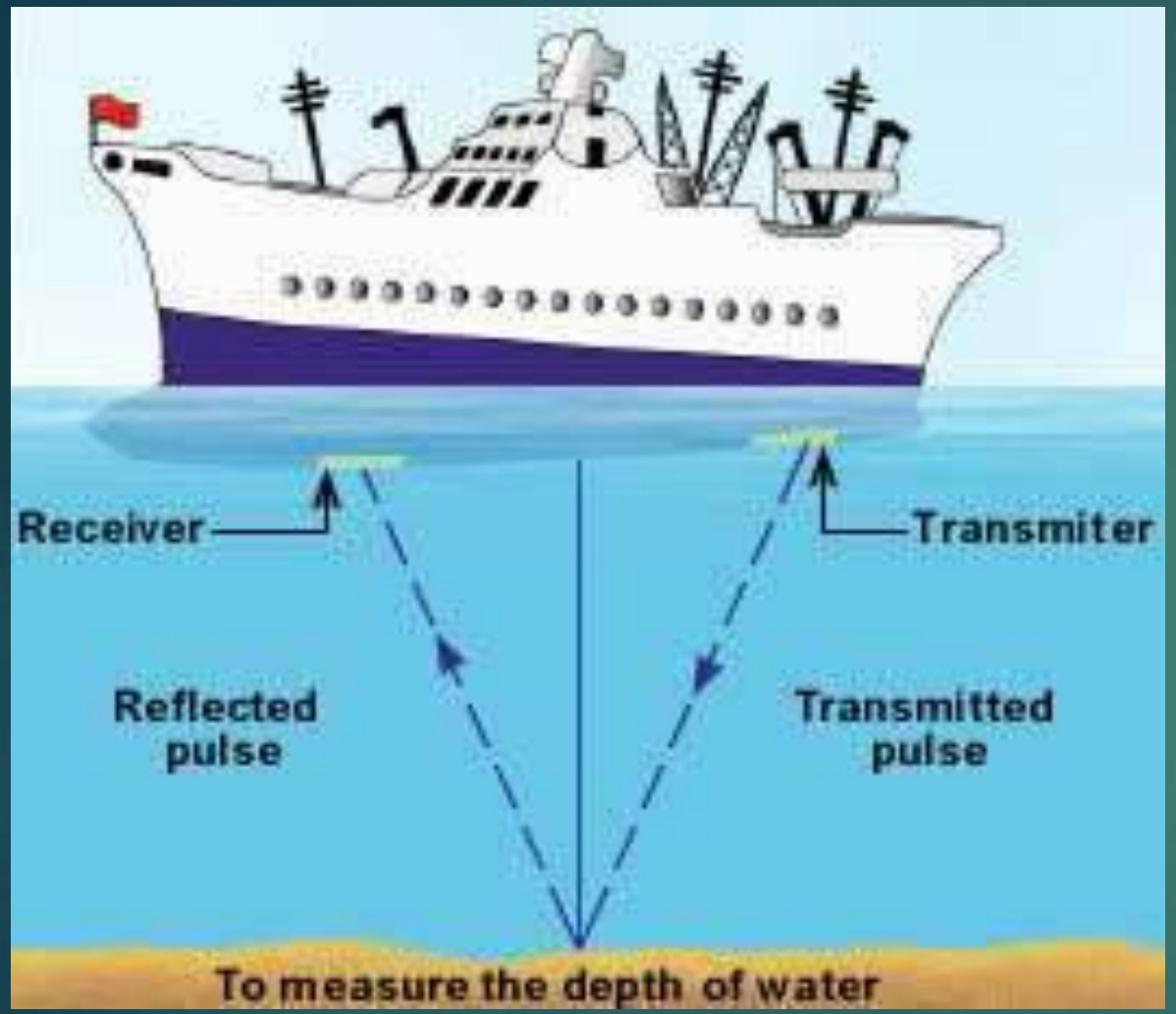


- But use of the sound by humans in the water is initially recorded by Leonardo da Vinci in 1490: a tube inserted into the water was said to be used to detect vessels by placing an ear to the tube.
- Sonar was first patented by Lewis Richardson and German physicist Alexander Behm in 1913.



Sonar

- Sonar is a device that is used to detect underwater objects using sound waves.
- In this system a sound pulse is generated and sent underwater through a transmitter.
- sound waves are reflected by the underwater object which are received at receiver.
- The time taken by sound wave to come back is recorded.
- And by knowing the speed of sound wave in water the distance can be easily calculated by formula.
- Distance = speed x time


Receiver
Transmiter
Reflected pulse
Transmitted pulse
To measure the depth of water

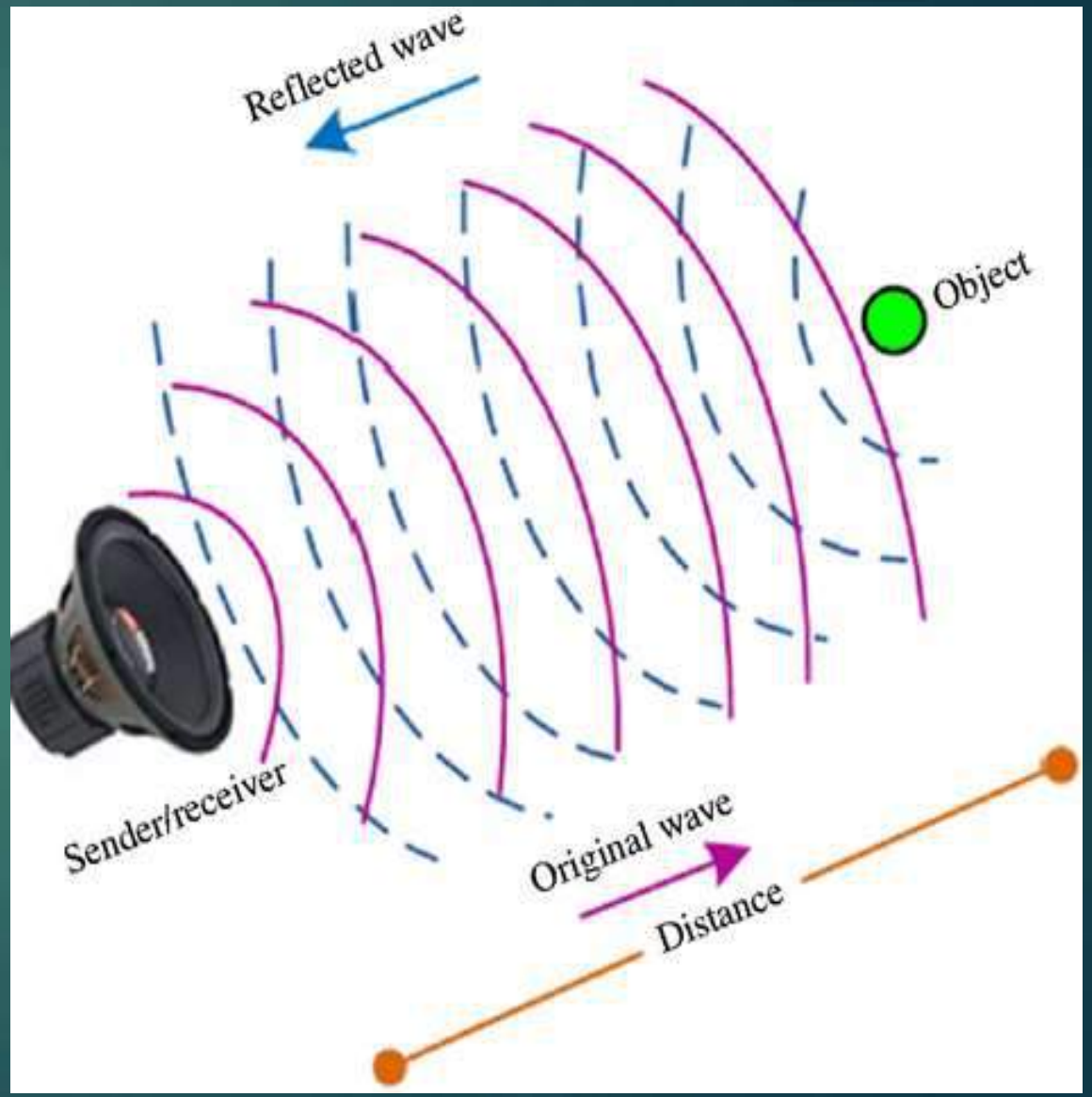
Type of sonar

sonar is of two types:

- Active sonar
- Passive sonar

Active sonar

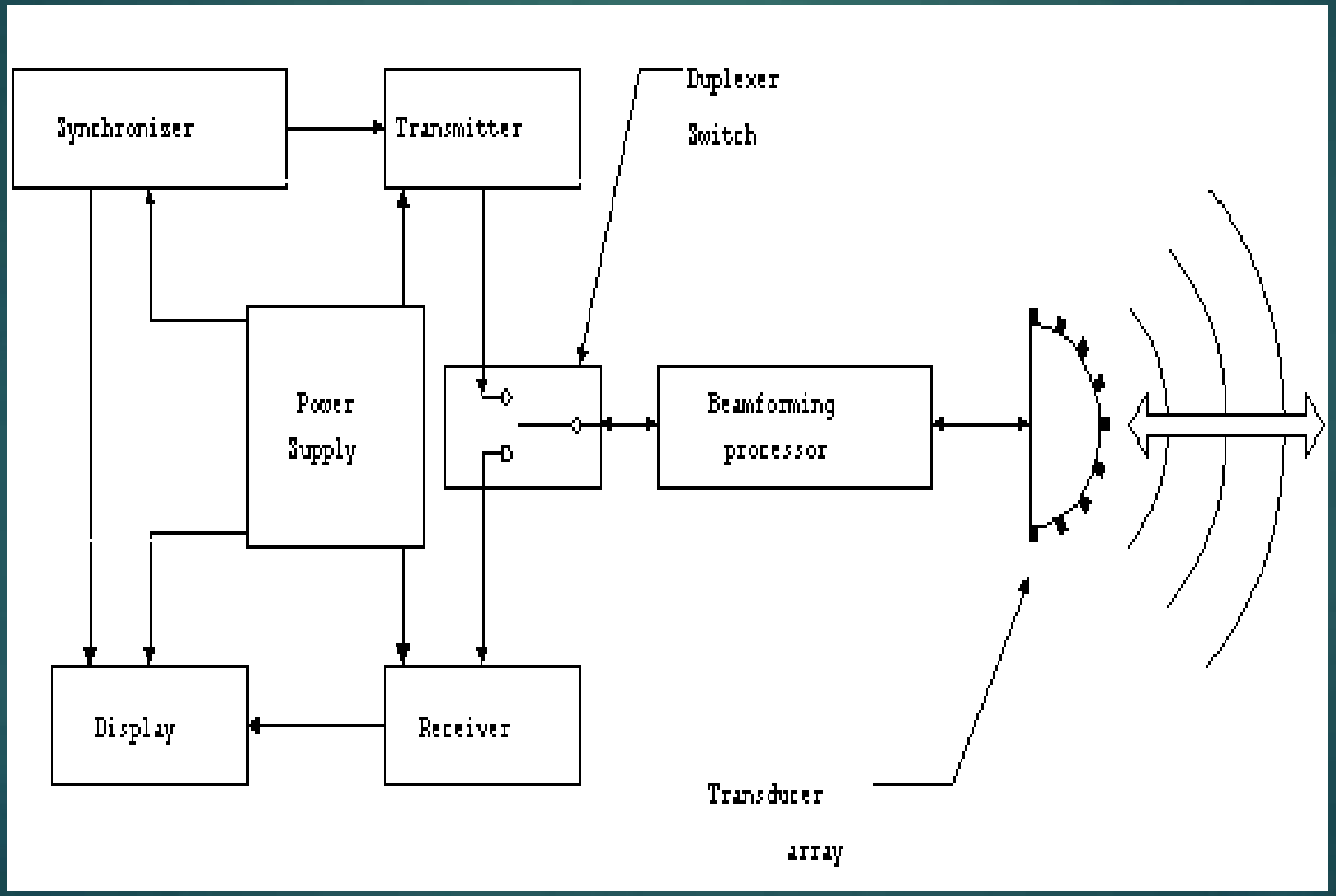
- Active sonar uses sound transmitter and receiver . And there are 3 modes of operation :
- Monostatic mode
- Bistatic mode
- Multistatic mode



- Monostatic mode : when the transmitter and receiver are at the same place.
- Bistatic mode : when the transmitter and receiver are separated by some distance.
- Multistatic mode : When more transmitters (or more receivers) are used, again spatially separated.

- Most sonars are used monostatically with the same array often being used for transmission and reception.
- Active sonar creates a pulse of sound, often called a "ping", and then listens for reflections (echo) of the pulse.
- This pulse of sound is generally created electronically using a sonar projector consisting of a signal generator, power amplifier and electro-acoustic transducer/array.
- To measure the distance to an object, the time from transmission of a pulse to reception is measured and converted into a range by knowing the speed of sound.
- To measure the bearing, several hydrophones are used, and the set measures the relative arrival time to each.

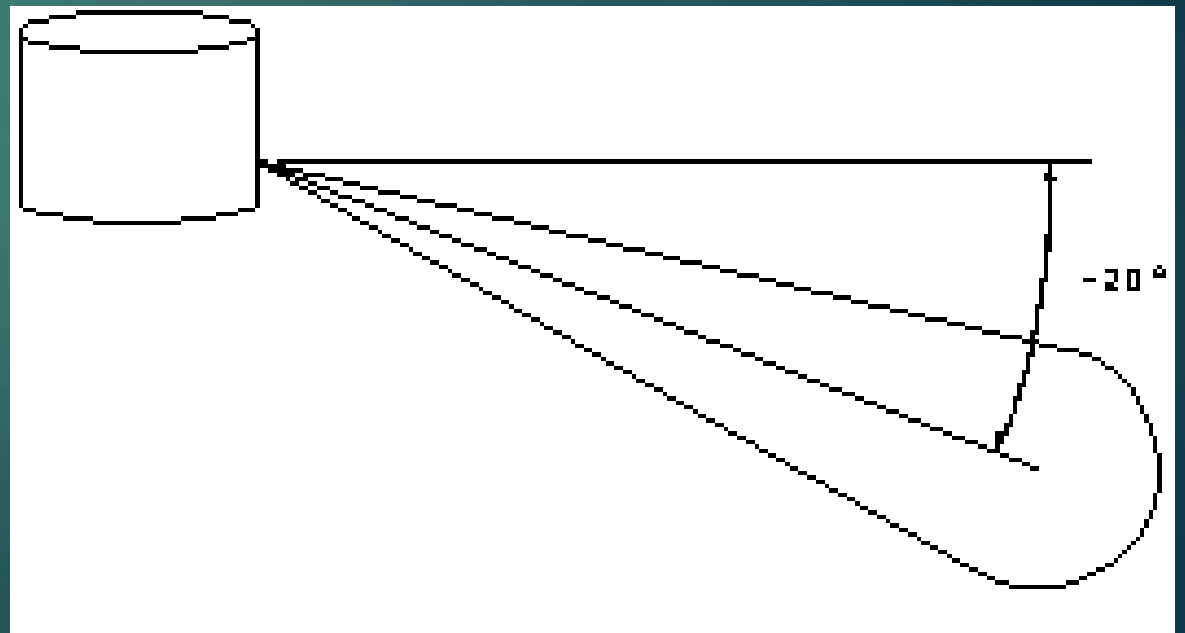
Block diagram of an active sonar



Functional components

- Transmitter : The transmitter generates the outgoing pulse. It determines pulse width,pulse reception frequency, modulation and carrier frequency.
- Transducer array : The individual transducers are simple elements with little or no directionality. They are arranged in an array to improve the directivity index, which improves the figure-of-merit by noise reduction.
- The array of transducers reduces the beamwidth in the horizontal direction, and is usually circular in order to give more or less complete coverage

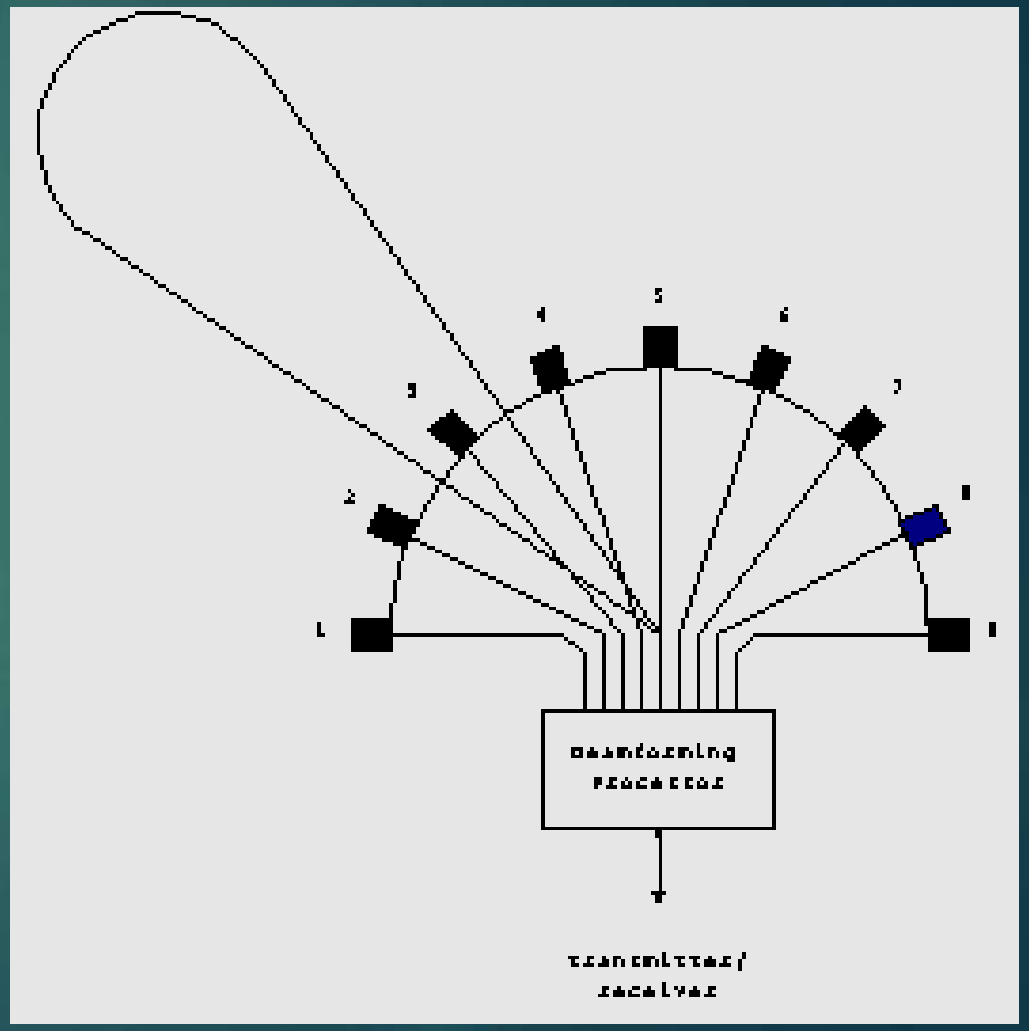
Vertical beam of typical transducer array.



Beamforming processor :

- The input/output of each transducer is put through a ,beamforming processor which applies time delays or phase shifts to each of the signals in such a way as to create a narrow beam in a particular direction.

- The width of the beam formed by the beamforming processor will determine the bearing accuracy of the system when searching.

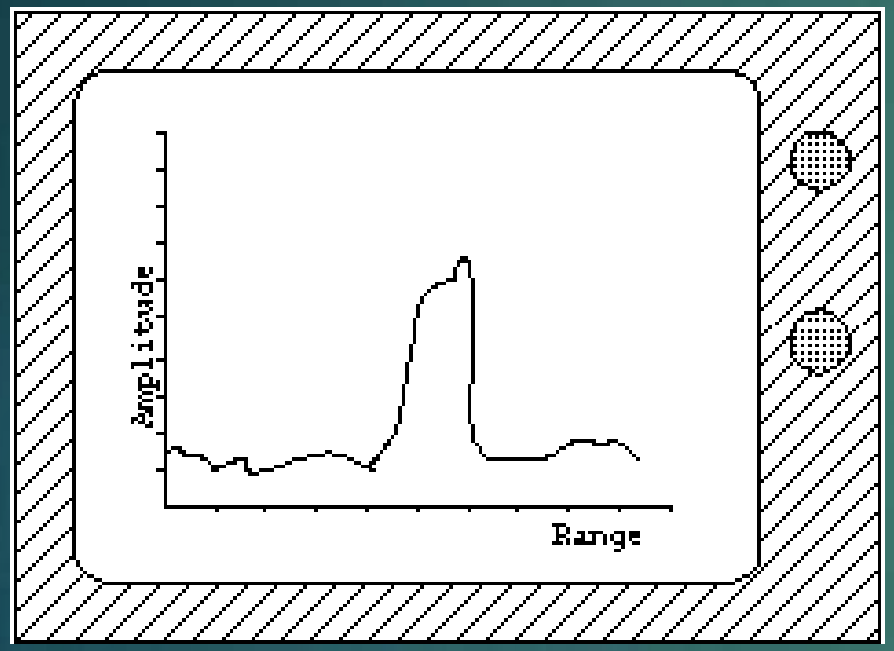


- Duplexer switch : it is a switch that toggles between transmitter and receiver.
- Syncroniser : Provides overall coordination and timing for the system. Reset the display for each new pulse in order to make range measurements.
- Receiver : Collects the received energy. The receiver may also demodulate the return if frequency modulation is used on transmission

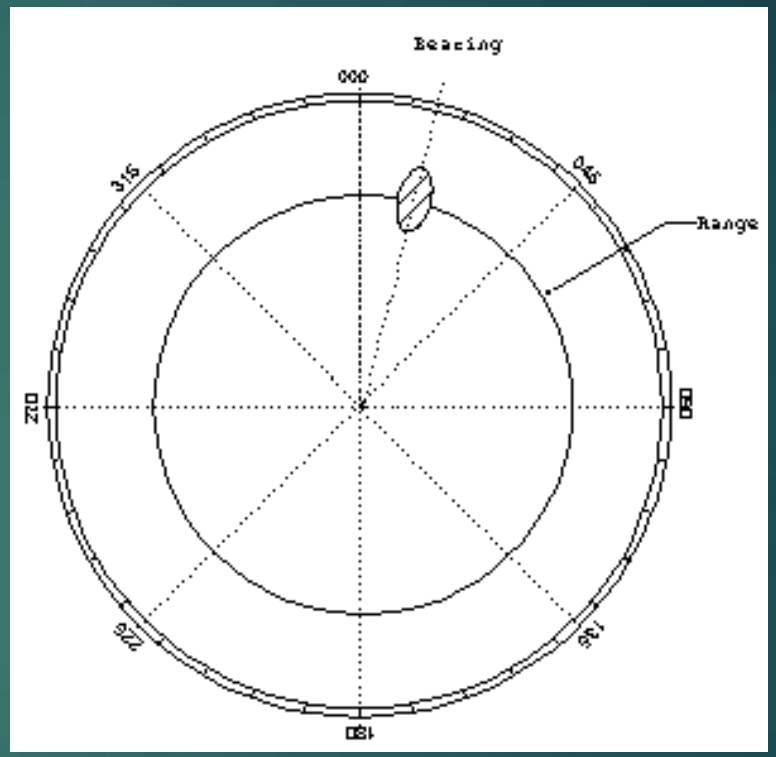
- Display : Puts all of the detection information into a visual format. There are several types:

- A-scan : the signal along a single beam for a portion of the listening cycle. A target appears as a raised section if it is in the beam.

- PPI(plan position indicator) : A top-down (geographic view). The sonar system must sequentially search individual beams which are displayed in their true or relative form. The strength of the return is represented by the intensity on the display.



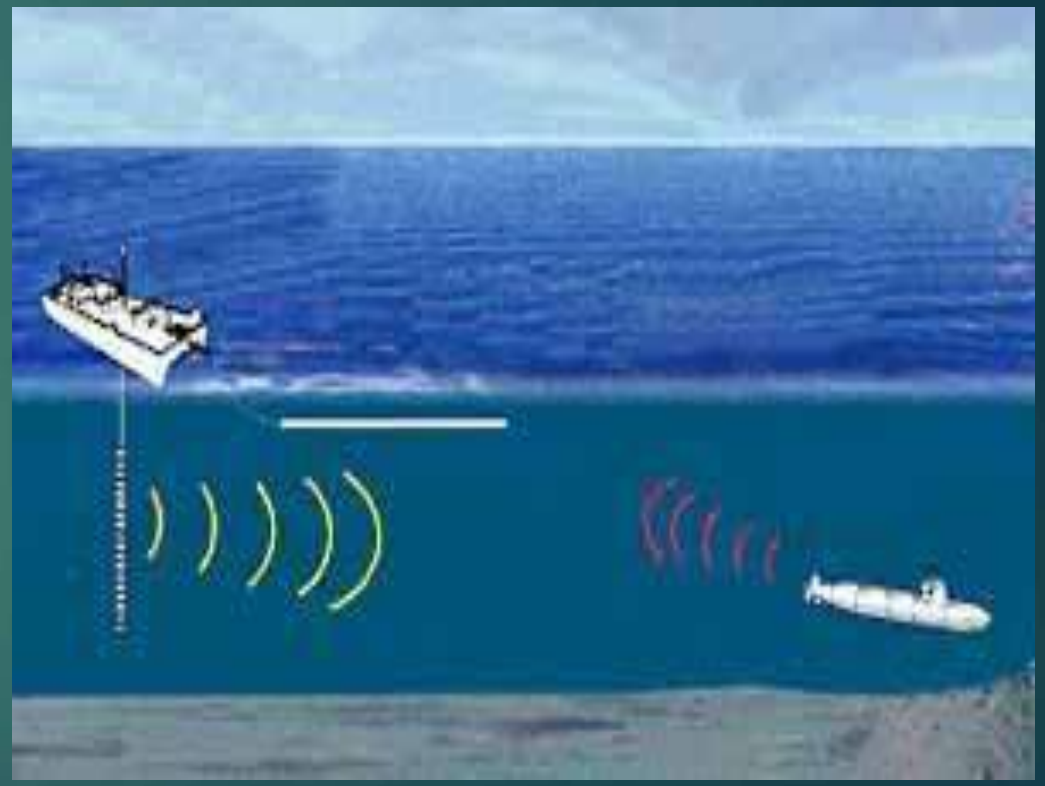
A – scan display



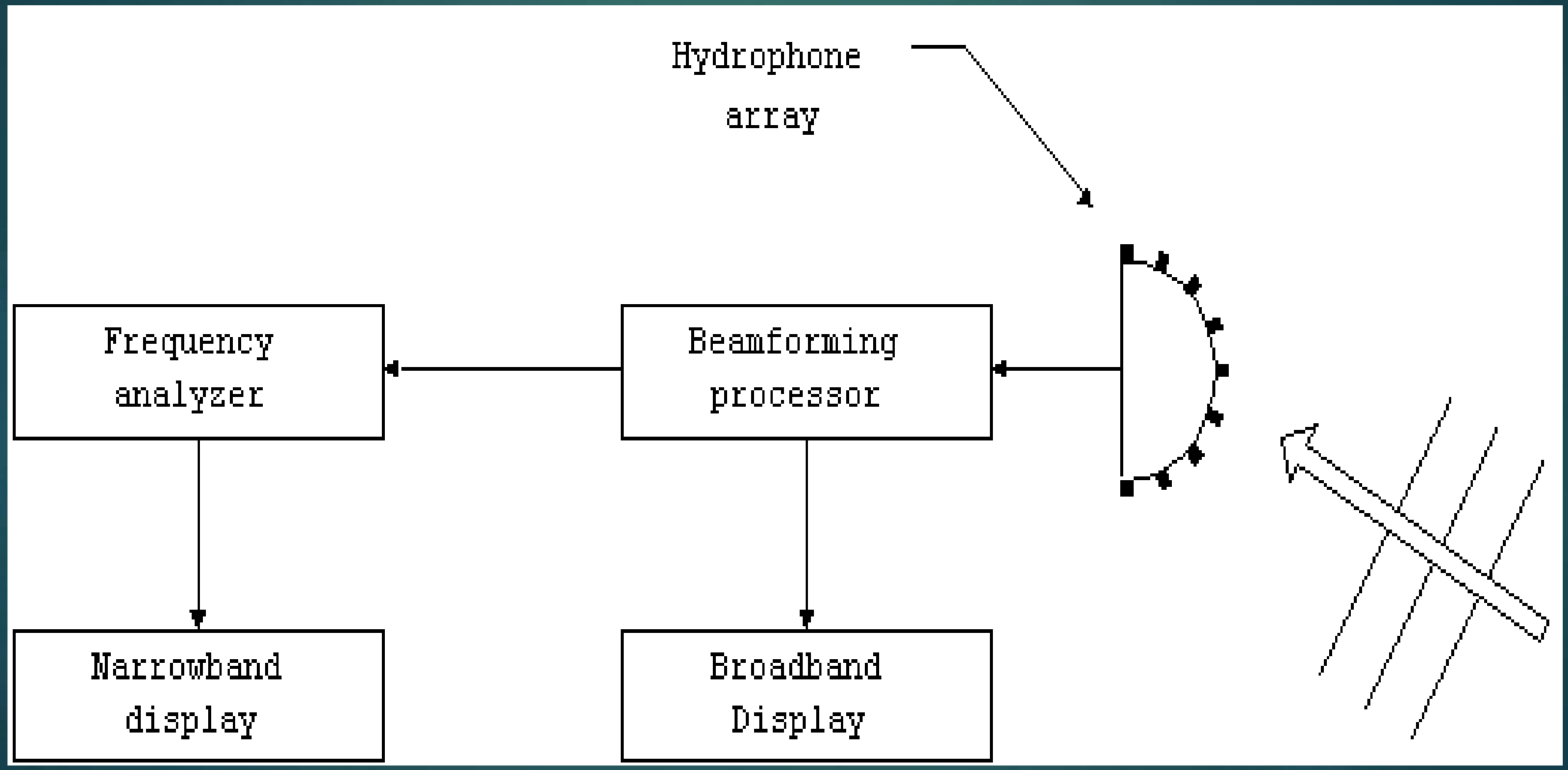
PPI display

Passive sonar

- Passive sonar listens without transmitting.
- Passive sonar has a wide variety of techniques for identifying the source of a detected sound.
- Passive sonar system have large sonic database but sonar operator classify signals by use of computer and use these databases to identify classes of ships and action.

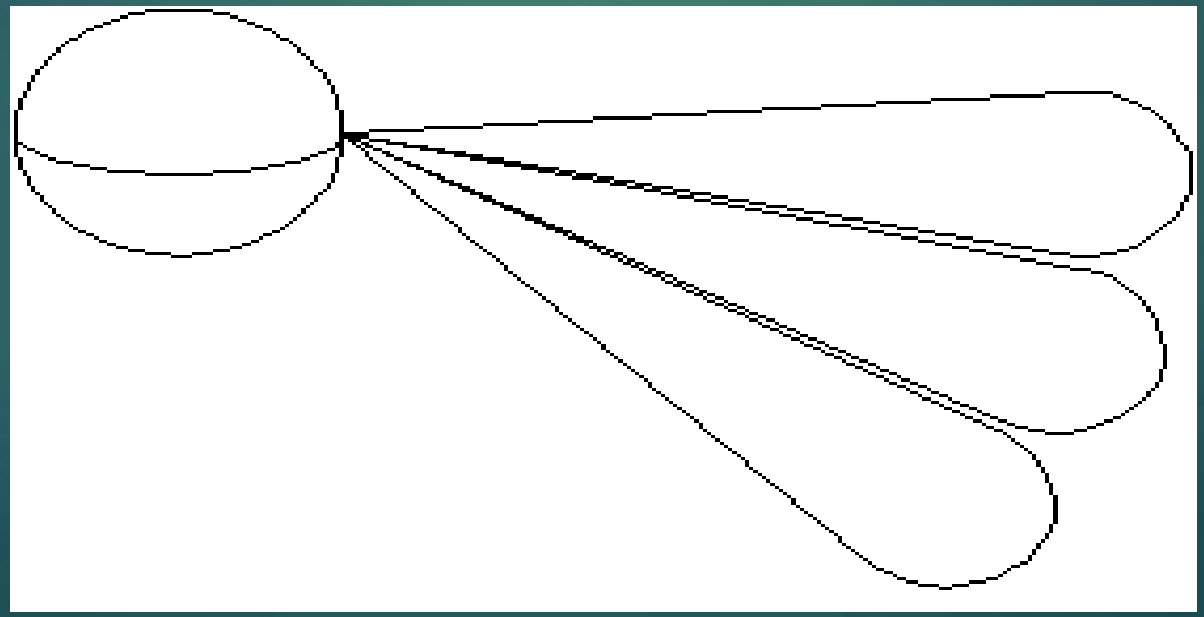


Block diagram of passive sonar

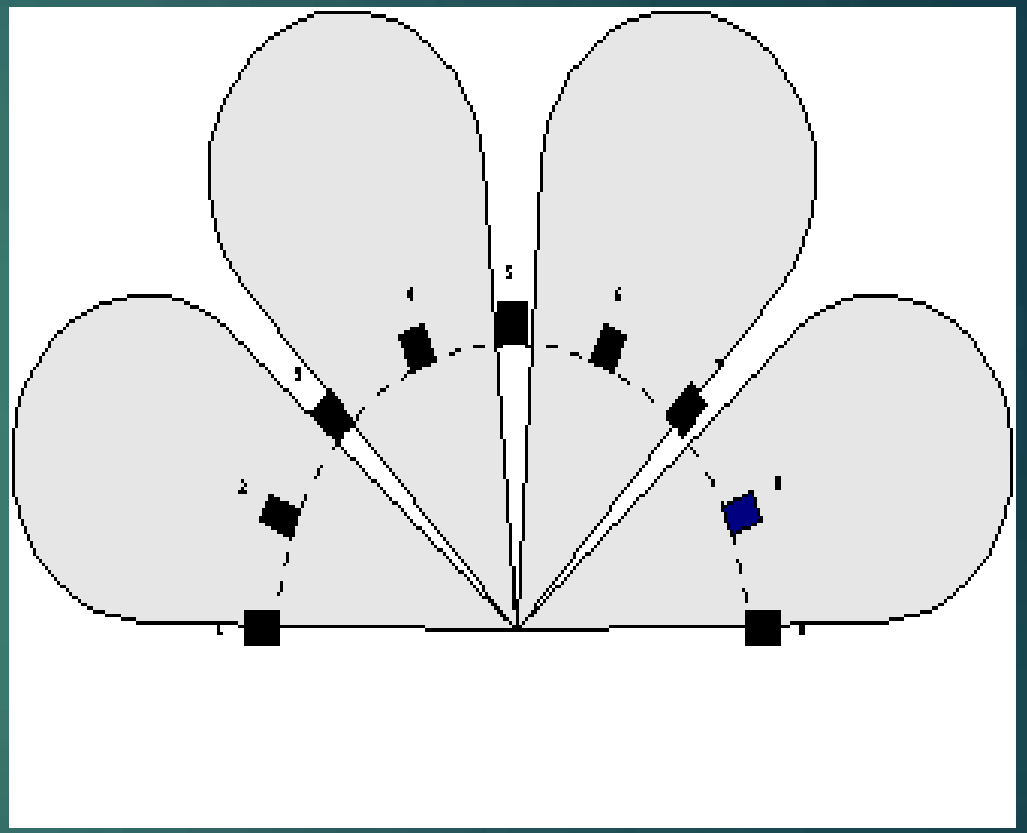


Functional components

- Hydrophone array : These are the sensitive elements which detect the acoustic energy emitted from the target. Again, they are arranged into an array to improve the beamwidth.
- The cylindrical array operates at a fixed vertical angle, usually downward.The large downward angles are only used for bottom bounce detection

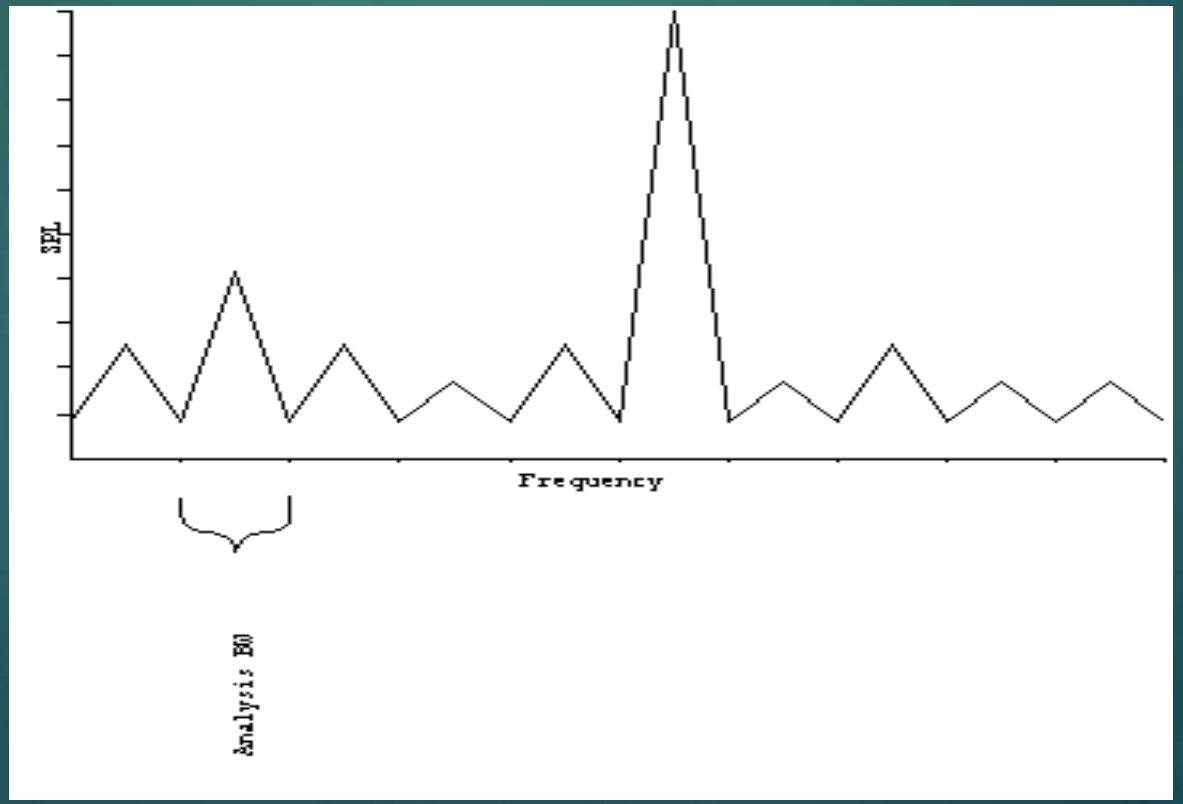


- Beamforming processor : the passive system must listen to all angles at all times. This requires a very wide beamwidth. The passive beamforming processor applies a unique set of time delays/phase shifts to the signal to create a particular beam. The difference in a passive system is that this process is repeated several times, each with a different set of time delays/phase shifts, in order to listen to many narrow beams nearly simultaneously.



- Frequency Analyzer :

The frequency analyzer breaks the signal into separate frequencies. This is the spectrum of the signal. For processing purposes, the frequencies are divided into small bands known as frequency bins. The width of each bin is called the analysis bandwidth.



Performance factor

- Sound propagation : Sonar operation is affected by variations in sound speed, particularly in the vertical plane. Sound travels more slowly in fresh water than in sea water. The speed is determined by the water's bulk modulus and mass density. The bulk modulus is affected by temperature, dissolved impurities (usually salinity), and pressure.
- Speed = 4388 + (11.25 × temperature (in °F)) + (0.0182 × depth (in feet)) + salinity (in parts-per-thousand).

application

- It is used to find the actual depth of the sea.
- Sonar systems are used to find lost ships and submarines.
- These are used in ocean surveillance systems.
- They are used by navy detect the locations of enemy submarines.
- They are used for under water security.

limitation

- It has an adverse effects on marine animals like dolphins and whales ,that also use sound waves for their navigation.
- It leads whales to painful and often fatal decompression sickness.
- The sonar systems generate lot of noise
- High intensity sonar sounds can create a small temporary shift in the hearing threshold of some fish

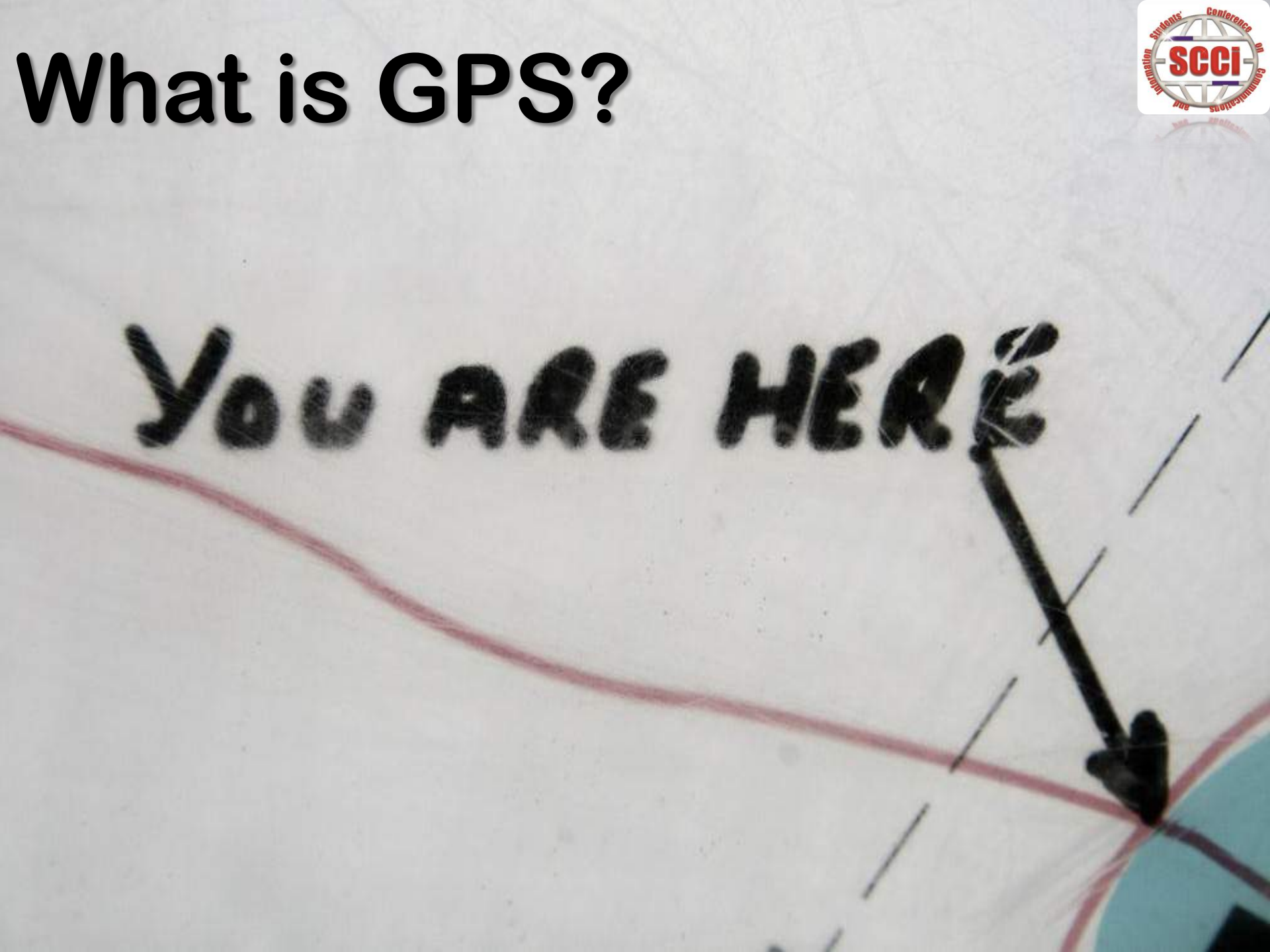
Global Positioning System (GPS)

A system that's changed navigation forever.

We will talk about:

- What is GPS?
- Why GPS?
- How GPS works?
- Real world applications of GPS.

What is GPS?



Why GPS?

Trying to figure out where you are and where you're going is probably one of man's oldest pastimes.

Why GPS?

Navigation and positioning are crucial to so many activities and yet the process has always been quite difficult and slow.

Finally

- Finally, the U.S. Department of Defense decided that the military had to have a super precise form of worldwide positioning.
- The result is the Global Positioning System, a system that's changed navigation forever.

How it works?

How GPS works?

1. Trilateration.
2. Measuring distance.
3. The perfect timing.
4. Position of satellites.
5. Error correction.

1-Trilateration

- More generally, trilateration methods involve the determination of absolute or relative locations of points by measurement of distances, using the geometry of Spheres or Triangles.

2- Measuring distance

- A GPS receiver measures distance using the travel time of radio signals.
- The whole thing boils down to those math problems we did in high school "velocity times travel time".
- As in the example:

Velocity (60 mph) x Time (2 hours) = Distance (120 miles).

3- The perfect timing

- If the timing of the radio signals is off by just a thousandth of a second, at the speed of light, that translates into almost 200 miles of error!

- On the satellite side, timing is almost perfect because they have incredibly precise atomic clocks on board.

4- Position of satellites

- On the ground all GPS receivers have an almanac programmed into their computers that tells them where in the sky each satellite is, moment by moment.

- The basic orbits are quite exact but just to make things perfect the GPS satellites are constantly monitored by the Department of Defense.

5- Error correction

- In the real world there are lots of things that can happen to a GPS signal that will make its life less than mathematically perfect.

- To get the most out of the system, a good GPS receiver needs to take a wide variety of possible errors into account.

Applications of GPS

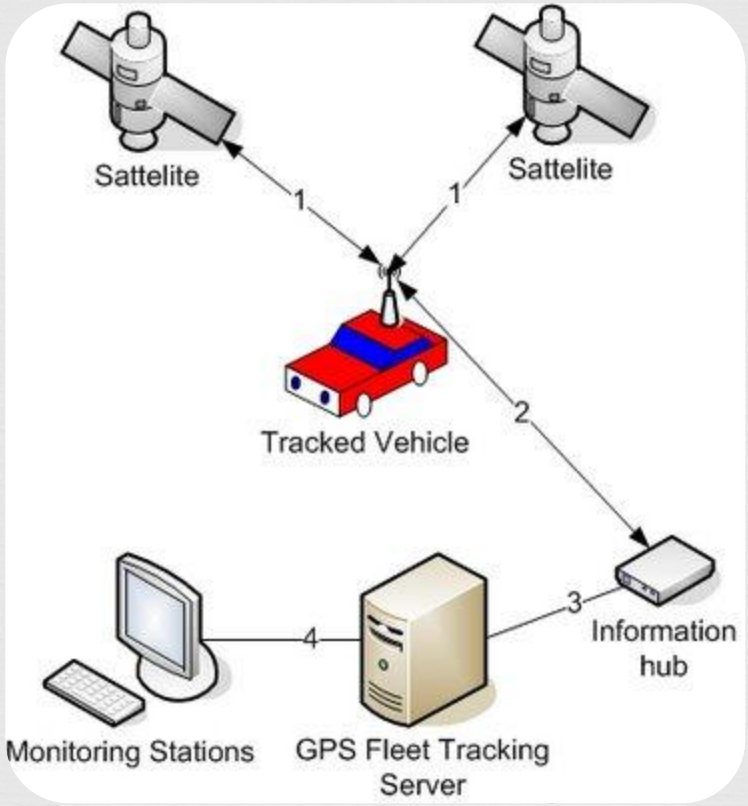
Location

GPS is the first positioning system to offer highly precise location data for any point on the planet, in any weather.

Navigation

- GPS helps you determine exactly where you are, but sometimes important to know how to get somewhere else.

Tracking



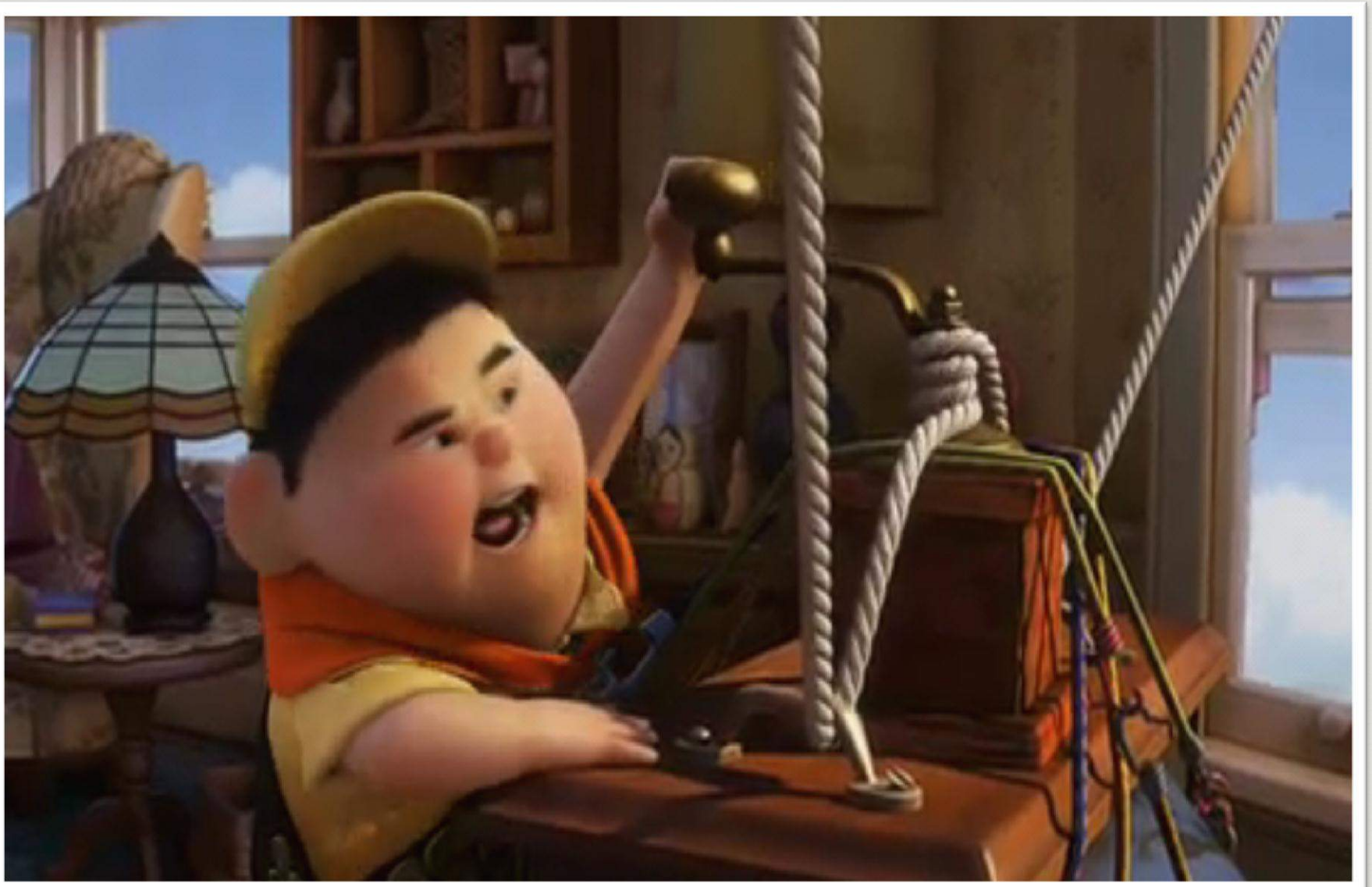
- If navigation is the process of getting something from one location to another, then tracking is the process of monitoring it as it moves along.

Mapping

- It's a big world out there, and using GPS to survey and map it precisely saves time and money in this most stringent of all applications.

Timing

- Knowing that a group of timed events is perfectly synchronized is often very important. GPS makes the job of "synchronizing our watches" easy and reliable.



Thank you

Mostafa Hussien

2.2 ADDRESSING MODES

Various methods of accessing the data are called addressing modes.

8051 addressing modes are classified as follows.

1. Immediate addressing.
2. Register addressing.
3. Direct addressing.
4. Indirect addressing.
5. Relative addressing.
6. Absolute addressing.
7. Long addressing.
8. Indexed addressing.
9. Bit inherent addressing.
10. Bit direct addressing.

1. ***Immediate addressing.***

In this addressing mode the data is provided as a part of instruction itself. In other words data immediately follows the instruction.

```
Eg.   MOV A,#30H
      ADD A, #83          # Symbol indicates the data is immediate.
```

2. ***Register addressing.***

In this addressing mode the register will hold the data. One of the eight general registers (R0 to R7) can be used and specified as the operand.

```
Eg.   MOV A,R0
      ADD A,R6
```

R0 – R7 will be selected from the current selection of register bank. The default register bank will be bank 0.

3. ***Direct addressing***

There are two ways to access the internal memory. Using direct address and indirect address. Using direct addressing mode we can not only address the internal memory but SFRs also. In direct addressing, an 8 bit internal data memory address is specified as part of the instruction and hence, it can specify the address only in the range of 00H to FFH. In this addressing mode, data is obtained directly from the memory.

```
Eg.   MOV A,60h
      ADD A,30h
```

4. ***Indirect addressing***

The indirect addressing mode uses a register to hold the actual address that will be used in data movement. Registers R0 and R1 and DPTR are the only registers that can be used as data pointers. Indirect addressing cannot be used to refer to SFR registers. Both R0 and R1 can hold 8 bit address and DPTR can hold 16 bit address.

```
Eg.   MOV A,@R0
      ADD A,@R1
      MOVX A,@DPTR
```

5. ***Indexed addressing.***

In indexed addressing, either the program counter (PC), or the data pointer (DTPR)—is used to hold the base address, and the A is used to hold the offset address. Adding the value of the base address to the value of the offset address forms the effective address. Indexed addressing is used with JMP or MOVC instructions. Look up tables are easily implemented with the help of index addressing.

```
Eg.   MOVC A, @A+DPTR    // copies the contents of memory location pointed by the sum of the
      accumulator A and the DPTR into accumulator A.
      MOVC A, @A+PC      // copies the contents of memory location pointed by the sum of the
      accumulator A and the program counter into accumulator A.
```

6. ***Relative Addressing.***

Relative addressing is used only with conditional jump instructions. The relative address, (offset), is an 8 bit signed number, which is automatically added to the PC to make the address of the next instruction. The 8 bit signed offset value gives an address range of +127 to —128 locations. The jump destination is usually specified using a label and the assembler calculates the jump offset accordingly. The advantage of relative addressing is that the program code is easy to relocate and the address is relative to position in the memory.

```
Eg.   SJMP LOOP1
      JC BACK
```

7. ***Absolute addressing***

Absolute addressing is used only by the AJMP (Absolute Jump) and ACALL (Absolute Call) instructions. These are 2 bytes instructions. The absolute addressing mode specifies the lowest 11 bit of the memory address as part of the instruction. The upper 5 bit of the destination address are the upper 5 bit of the current program counter. Hence, absolute addressing allows branching only within the current 2 Kbyte page of the program memory.

```
Eg.   AJMP LOOP1
      ACALL LOOP2
```

8. ***Long Addressing***

The long addressing mode is used with the instructions LJMP and LCALL. These are 3 byte instructions. The address specifies a full 16 bit destination address so that a jump or a call can be made to a location within a 64 Kbyte code memory space.

```
Eg.   LJMP FINISH
      LCALL DELAY
```

9. ***Bit Inherent Addressing***

In this addressing, the address of the flag which contains the operand, is implied in the opcode of the instruction.

```
Eg.   CLR C   ;     Clears the carry flag to 0
```

10. ***Bit Direct Addressing***

In this addressing mode the direct address of the bit is specified in the instruction. The RAM space 20H to 2FH and most of the special function registers are bit addressable. Bit address values are between 00H to 7FH.

```
Eg.   CLR 07h     ;     Clears the bit 7 of 20h RAM space
      SETB 07H    ;     Sets the bit 7 of 20H RAM space.
```